Integration of Epitaxial Systems for Electronics Applications

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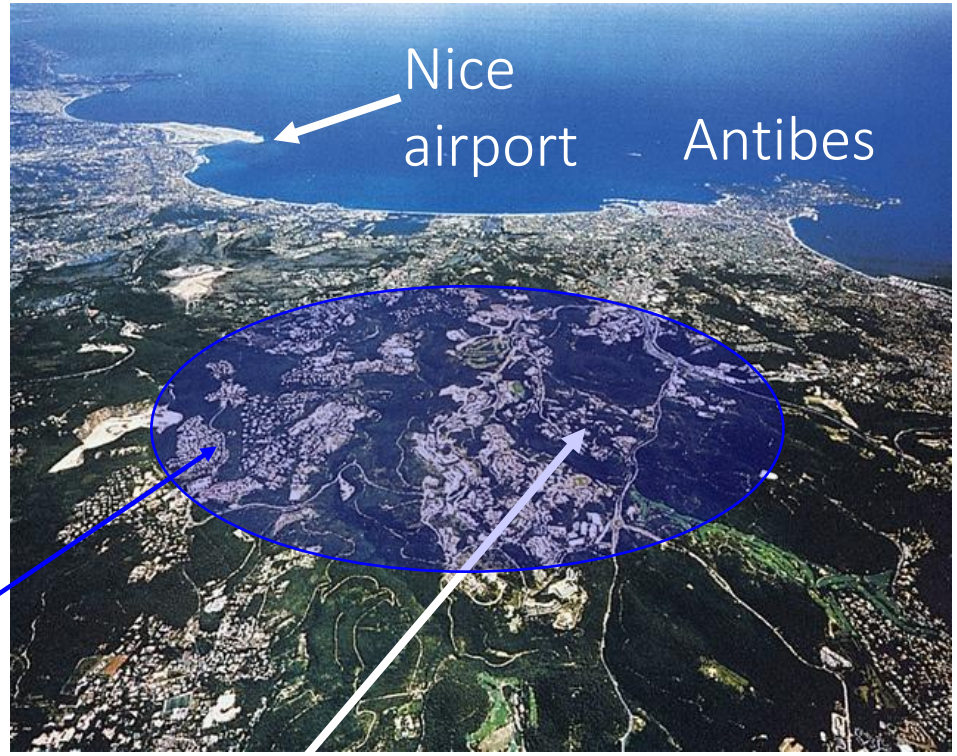
cnrs
dépasser les frontières

UNIVERSITÉ CÔTE D'AZUR

CRHEA



Sophia Antipolis: 30 000 jobs

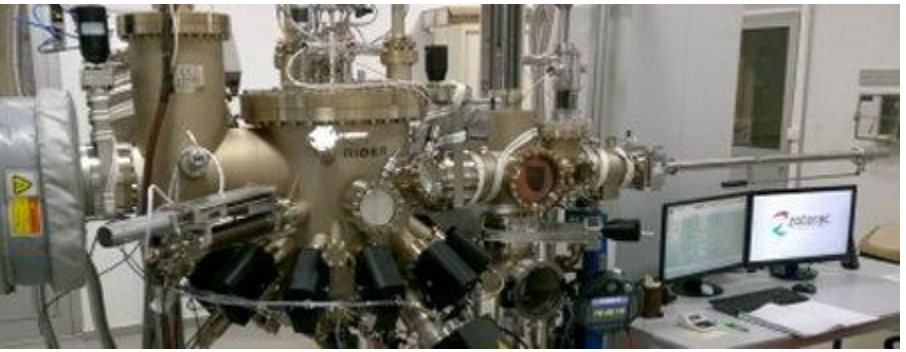
1200 companies / labs

- Research Labs (academic & private)
- Companies (medical, software, electronic, numerical related to telecoms…)

CRHEA: Research Center for Hetero-Epitaxy & Applications

(~ 60 pers., researchers, professors, students, engineers, administratives)

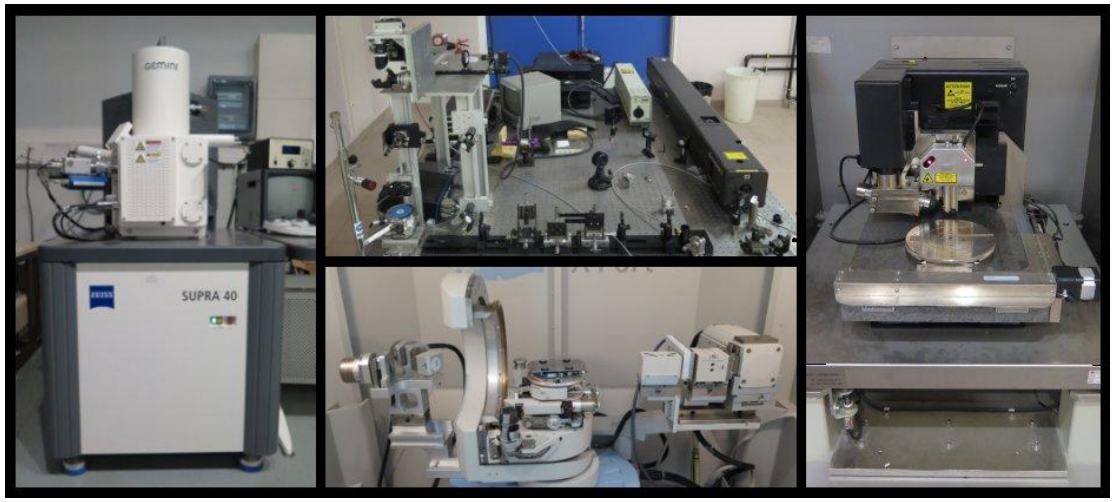
Activities



EPITAXY

Semiconductors

(MBE, MOCVD)



Optical Char.

PL, µ-PL, CL

Electrical Char.

(I-V, Hall, C-V)

Clean Room Devices

(LEDs, HEMTs)

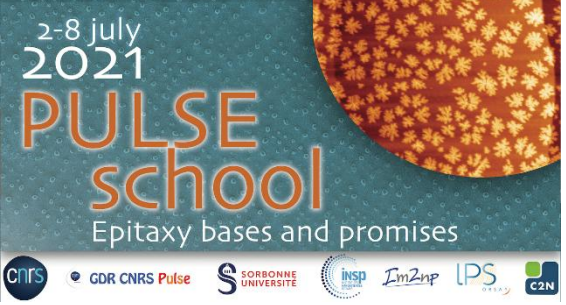
Structural Characterization

(X, AFM, SEM, TEM)

- **GaN :** LEDs, µ-cavities, µ-lasers, electronics (RF, power)
- **ZnO :** IR, THz (QWIP, QCL), µ-cavities (polaritons)
- **SiC :** power electronics, buffer for GaN, MEMS
- **Graphene & 2D materials :** CVD growth, VdW epitaxy
- **Metasurfaces:** µ- / nano-fabrication on nitrides, oxides

Outline

- **Si Electronics**
  - Si-based Technology: Field Effect Transistor, Metal-Oxide FET & CMOS Technology
  - From MOSFET to Integrated Circuits
  - Scaling: motivations & issues
- **Heterogeneous Integration & Defect Engineering**
  - Heterogeneous Material Integration on Si Platforms
  - From MOSFET to HEMT
  - Epitaxy Defect Engineering
- **SiGe & III-V technology**
  - Strained Si MOSFET
  - SiGe channels & III-V HEMTs
  - Nitride Materials – AlGaN/GaN HEMTs
- **Conclusions & perspectives**



Si Electronics

Si-based technology

➢ Why Si ?

Silicon: abundant (2nd element (28%) after oxygen (46%)), cheap and simple purification process:

Reduction:

Silicon dioxide (SiO_2) is reduced (@ 1500-2000 °C) : $\mathbf{SiO_2 + C \rightarrow Si + CO_2}$

⇒ Si is metallurgical grade silicon (MG-Si) 98-99% pure.

Presence of transition metals --> deep levels in the bandgap with high recombination activity --> unsuitable for use in electronics

https://www.pveducation.org/pvcdrom/manufacturing-si-cells/refining-silicon

Purification in 2 steps:

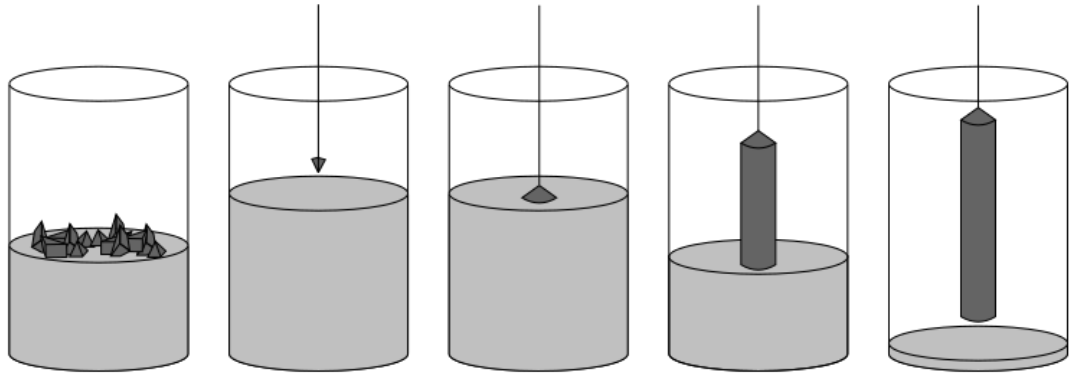
- MG-Si is reacted with anhydrous HCl (@ 300 °C) to form $SiHCl_3$: $\mathbf{Si + 3HCl \rightarrow SiHCl_3 + H_2}$
- $SiHCl_3$ is reacted with hydrogen (@ 1100°C) to produce a very pure Si : $\mathbf{SiHCl_3 + H_2 \rightarrow Si + 3\ HCl}$

Reaction inside large vacuum chambers & the Si is deposited onto thin polysilicon rods to produce high-purity polysilicon rods.

The resulting rods of semiconductor grade silicon are broken up to form the feedstock for the crystallisation process.

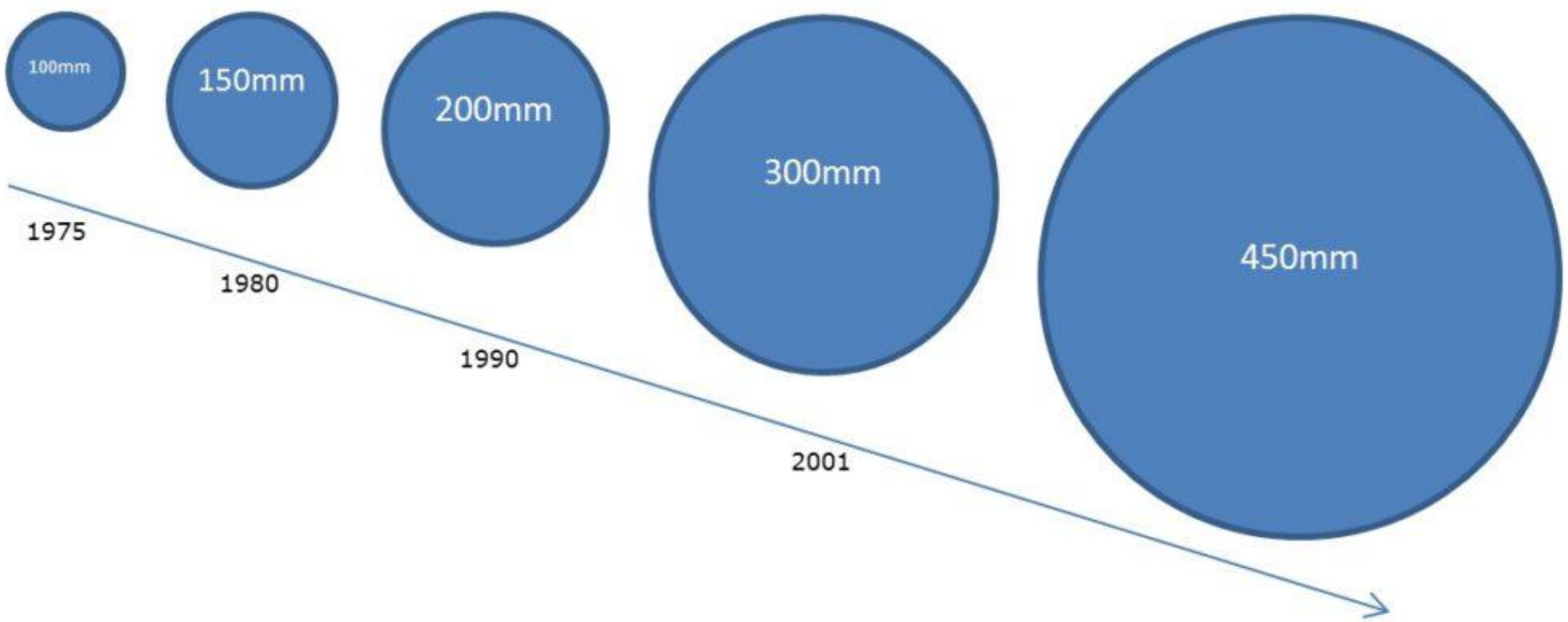
- Czochralski (CZ) process (Crystal pulling)

- Floating zone (FZ) process



Si wafers

- **Strong increase of the wafer diameter since the 1960's**
  from 100mm to 300 mm
  --> reduction of the price per transistor & performances improvement



Field Effect Transistor

- **Transistor = SC device used to amplify or switch electronic signals and electrical power**
- **A field effect transistor (FET) uses an electric field to control the flow of current & only one kind of charge carrier**

→ **Amplifier** = electronic device that can increase the power of a signal

→ **Switch** = electrical component that can disconnect or connect the conducting path in an electrical circuit

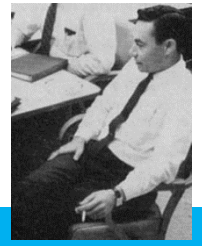
« concept of a field-effect transistor »
Julius Edgar Lilienfeld
(1882 – 1963)

First working device in 1947 by John Bardeen, Walter Brattain and William Shockley (Bell Labs)

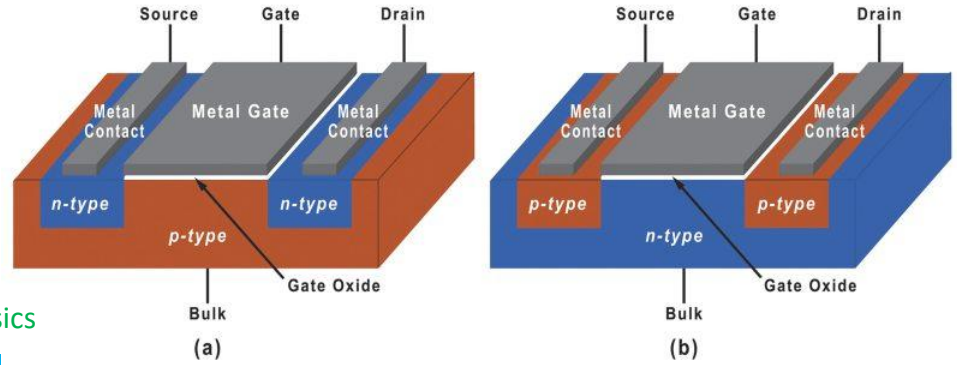
Nobel Prize in Physics in 1956

- **Main type of transistor used = metal–oxide semiconductor field-effect transistor (MOSFET)**

invented by Mohamed Atalla and Dawon Kahng (1959, Bell Labs)



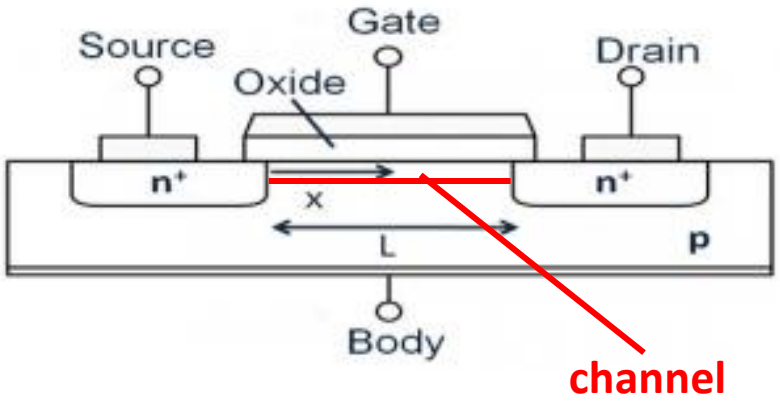
https://www.mksinst.com/n/mosfet-physics



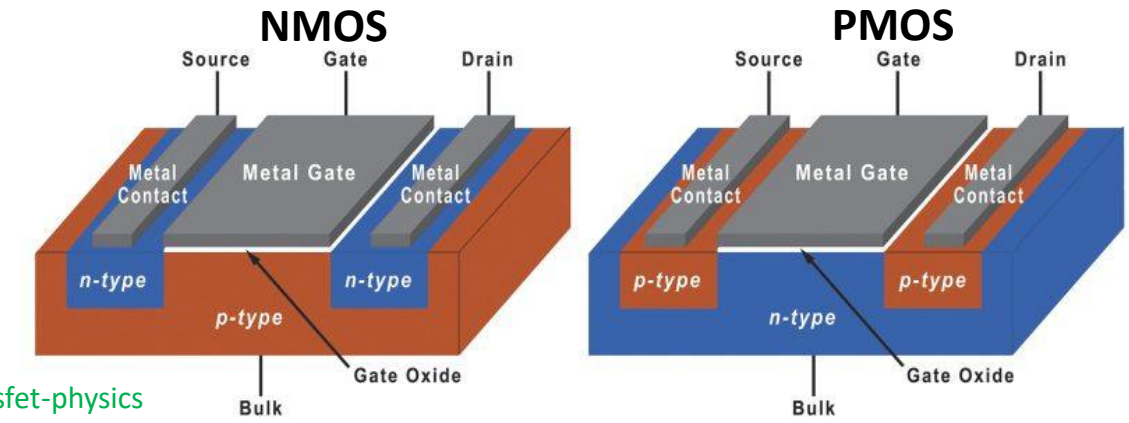
Metal–Oxide semiconductor FET (MOSFET)

- Basic MOSFET devices used metal as the gate material (now poly-Si), silicon dioxide as insulator (gate oxide) and Si as substrate.
  - The gate switches on and off by the transistor with an electric field crossing the gate oxide

https://www.elprocus.com/the-fabrication-process-of-cmos-transistor/



- **3 terminal device :**
  The Source, Gate, Drain and Body terminals. In general, the body is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor.
- **The functionality of MOSFET depends on the electrical variations in the channel along with the flow of carriers** (either holes or electrons).
  The charge carriers enter into the channel through the source and exit via the drain.
- **The N-Channel MOSFET** has an **N-channel region**
- **The P- channel MOSFET** has a **P- Channel region**



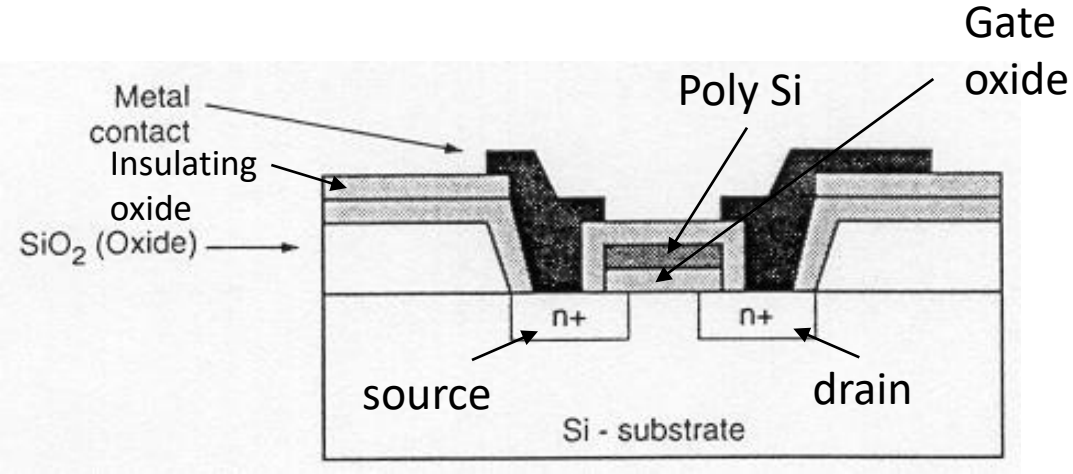
https://www.mksinst.com/n/mosfet-physics

Metal–Oxide semiconductor FET (MOSFET)

- **Depletion mode and enhancement mode are two major transistor types:**
  - depletion = transistor in a normally-ON state
  - enhancement = transistor in a normally-OFF state
  } **at zero gate-source voltage**

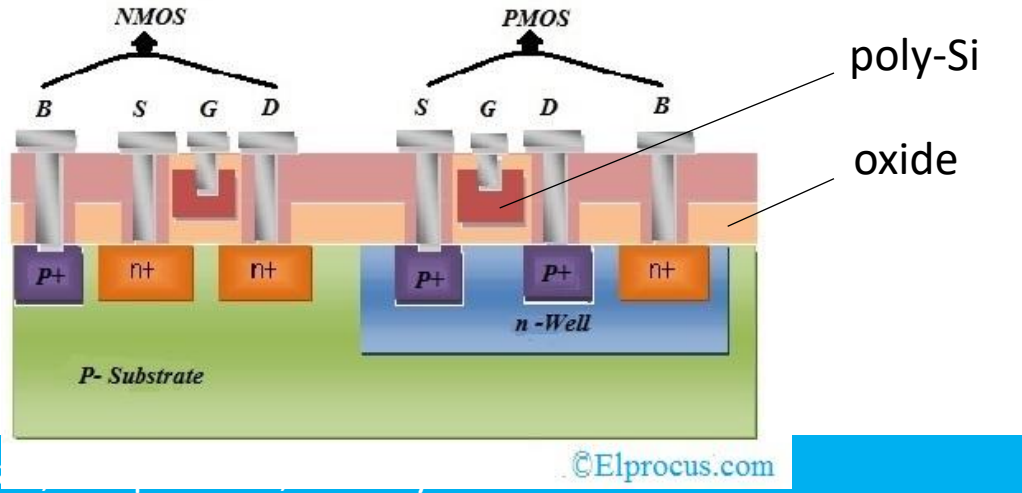
- **MOS Transistor main elements & process:**

1. oxidation of the silicon substrate (field oxide) + etching part of the SiO_2 ;
2. formation of a thin oxide layer (gate oxide–thermal oxidation) + **deposition of poly Si (by CVD);**
3. etching+doping (implantation) of Si → creation of the source & drain junctions (self-aligned proc.);
4. **insulating layer of SiO_2 (by CVD)** + etching (contact windows for source & drain) ;
5. deposition of the metal contact (Al) ;



http://emicroelectronics.free.fr/onlineCourses/VLSI/ch02.html

- **CMOS technology: complementary MOS technology using both N and P channel devices**

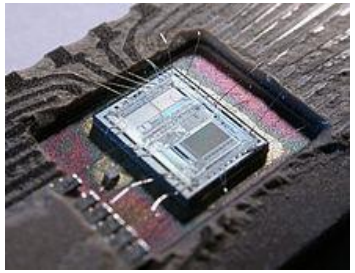
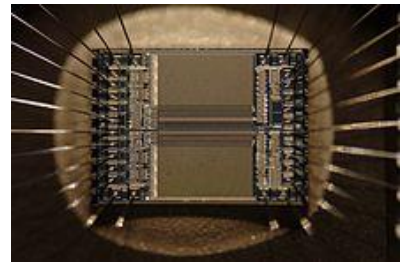


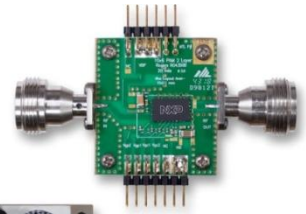
Complementary metal–oxide–semiconductor (CMOS)

- **Advantages of CMOS: high noise immunity & low static power consumption**

- CMOS technology is used to implement **logic gates and other digital circuits in integrated circuit (IC) chips,** such as microprocessors, microcontrollers, memory chips, and other digital logic circuits.

- CMOS technology is also used for **analog circuits** such as image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers for many types of communication.



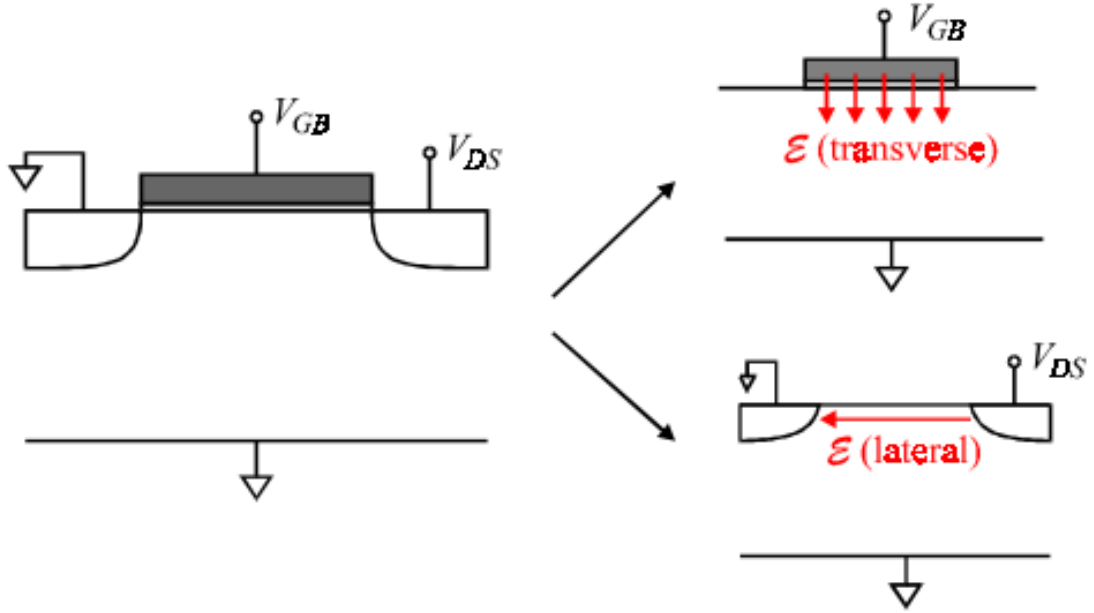

https://en.wikipedia.org/wiki/CMOS#Logic



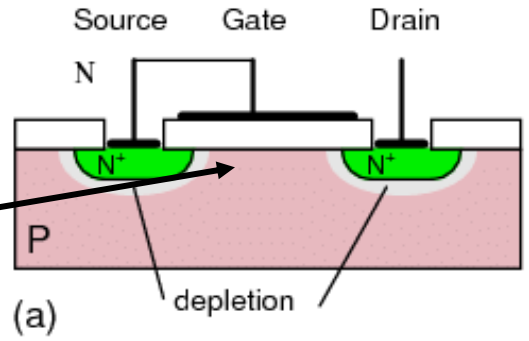


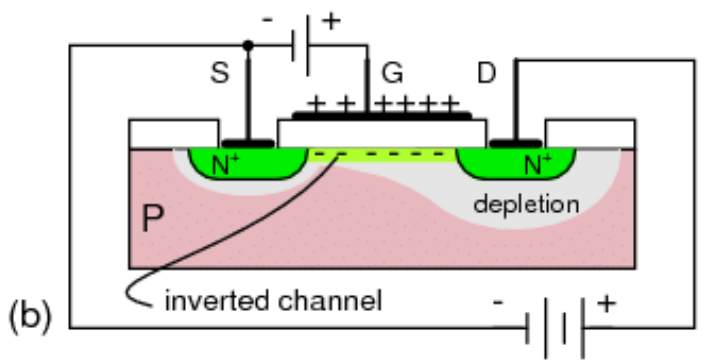

MOSFET Characteristics (basics)

- MOSFET are characterized by
  2 electric field distributions in the structure:
- **The transverse field caused by the potential difference between the gate and the source (V_{GS}). This field supports the substrate depletion region ($V_{GS} < V_{th}$) and inversion layer ($V_{GS} > V_{th}$).**
- **The lateral field from source to drain potential (V_{DS}) --> main mechanism for current flow in the MOSFET.**



A depletion region @ zero or low V_{GS}. No current flow through the channel.





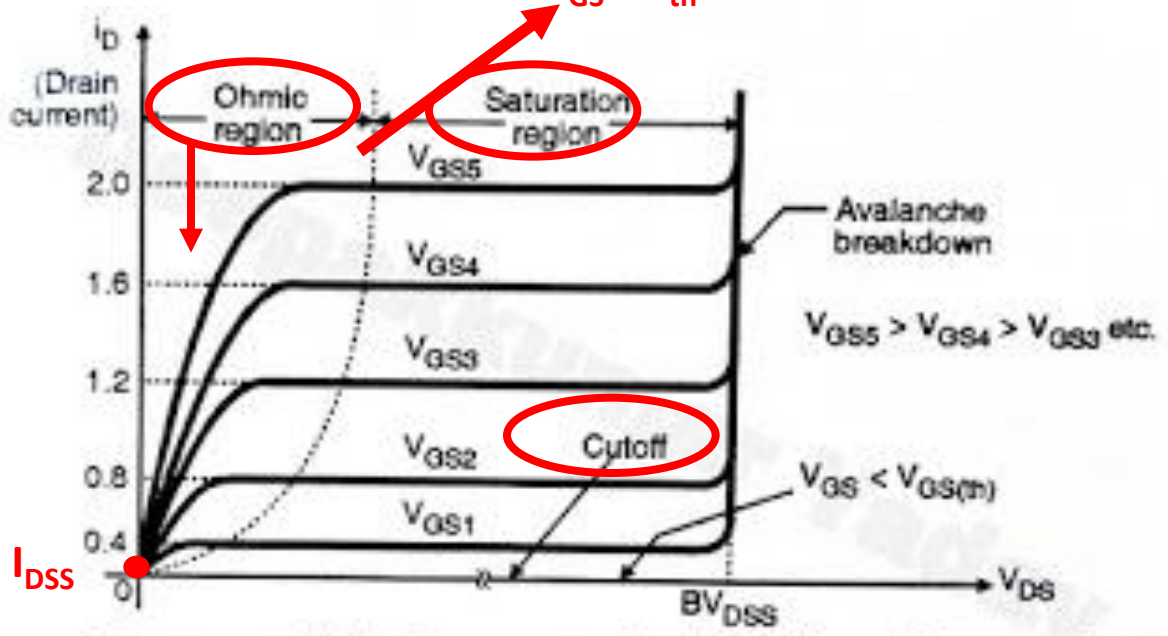
An inversion region with an excess of e- forms below the gate oxide. This region connects the source and drain N-type regions, forming a continuous N-region from source to drain.

MOSFET Characteristics (basics)

- **The output characteristics represents the drain current I_D vs. drain to source V_{DS} for different values of gate to source voltage V_{GS}** $V_{GS} - V_{th}$

- **The operation of MOSFET is used in 3 main regions:**
  - **Cut-off region:** the device will be in the OFF condition and NO current flow through it
  - **Linear/Ohmic region:** the current I_D increases linearly with the voltage V_{DS}
  - **Saturation region:** the drain to source current value I_D is constant & independent of V_{DS} (the channel is pinched off at the drain side)

A 4th region occurs as V_{DS} increases beyond V_{DSS} (saturation): the pinch off point moves away from the drain by ΔL and has the effect of changing the effective channel length in the transistor



Output IV characteristic of n channel enhancement mode VMOSFET

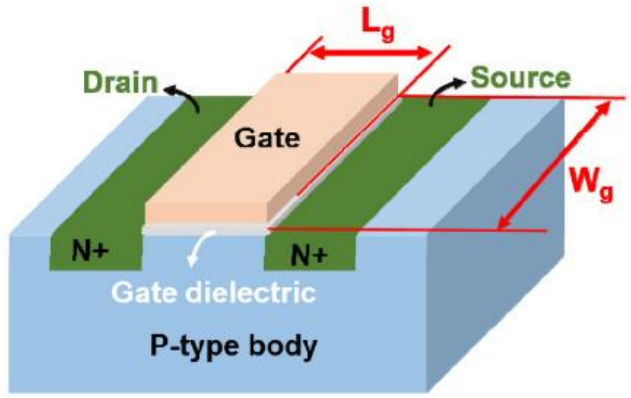
I_{DSS}: maximum current flowing through when the gate voltage V_{GS} is 0V.

MOSFET Characteristics (basics)

- **<u>Linear/Ohmic region:</u> In this region, the MOSFET works as an amplifier functionality. The ability of MOSFET to amplify the signal is given by the output/input ratio:**

--> transconductance $g_m = (dI_D/dV_{GS})_{VDS} = V_{DS}\mu WC_i/L$

μ = carrier mobility
L = gate length
W = gate width
C_i = gate insulator capacitance



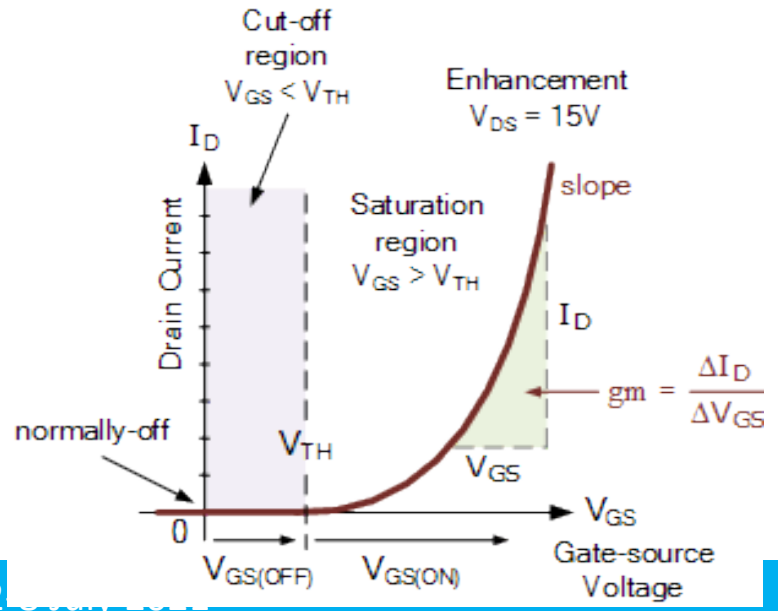
➡ **High transconductance is obtained with high values of:**

- **the low field electron mobility** (before saturation)
- **thin gate insulator layers**

(--> larger gate insulator capacitance $c_i = \varepsilon_i/d_i$ *with*

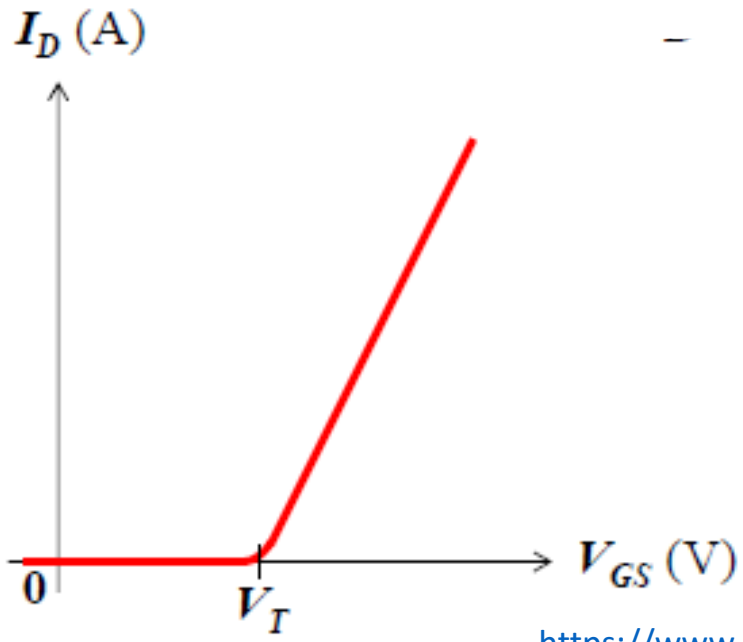
ε_i *the permittivity and* d_i *the thickness of the gate dielectric)*

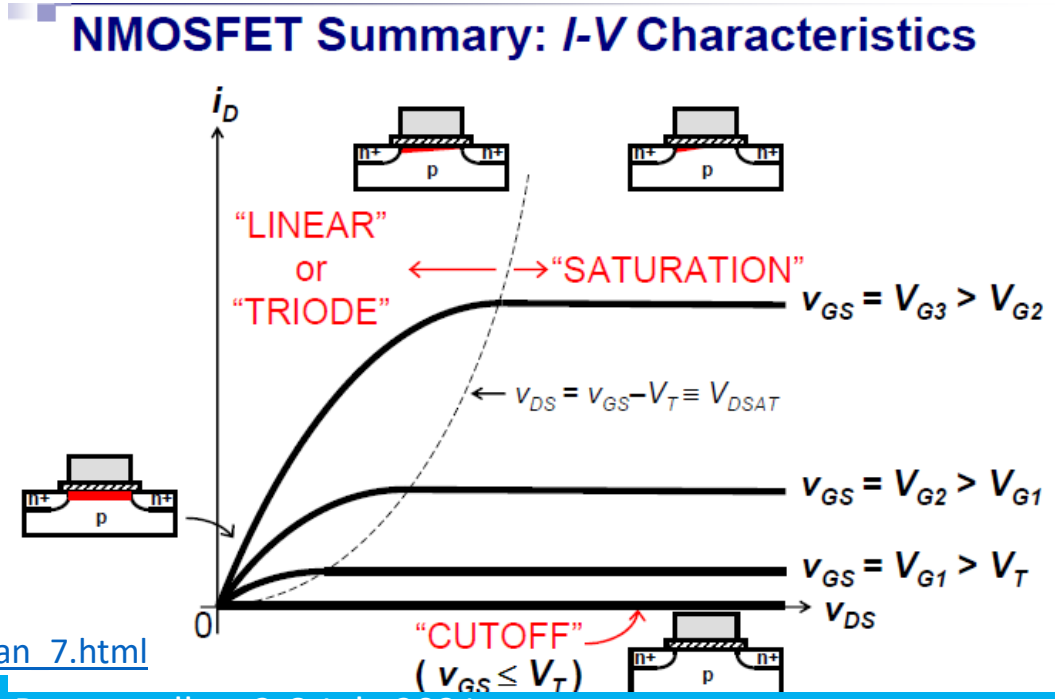
- **large *W/L ratios***



MOSFET Characteristics (basics)

- **MOSFET used as an electronic switch** (for controlling loads & in CMOS digital circuits). **They operate between the cut-off & saturation regions.**
- **Cut-off region:** V_{GS} is low or zero, the channel resistance is very high & the transistor acts like an open circuit --> no current flows through the channel. **The MOSFET is "OFF" operating.**
- **Saturation region:** The ON-state gate voltage V_{GS} ensures that the MOSFET is "ON" at a specific drain current I_D increases to its maximum value becomes constant independently of V_{DS} and depends only on V_{GS}. **The transistor is "ON" operating and behaves like a closed switch.**





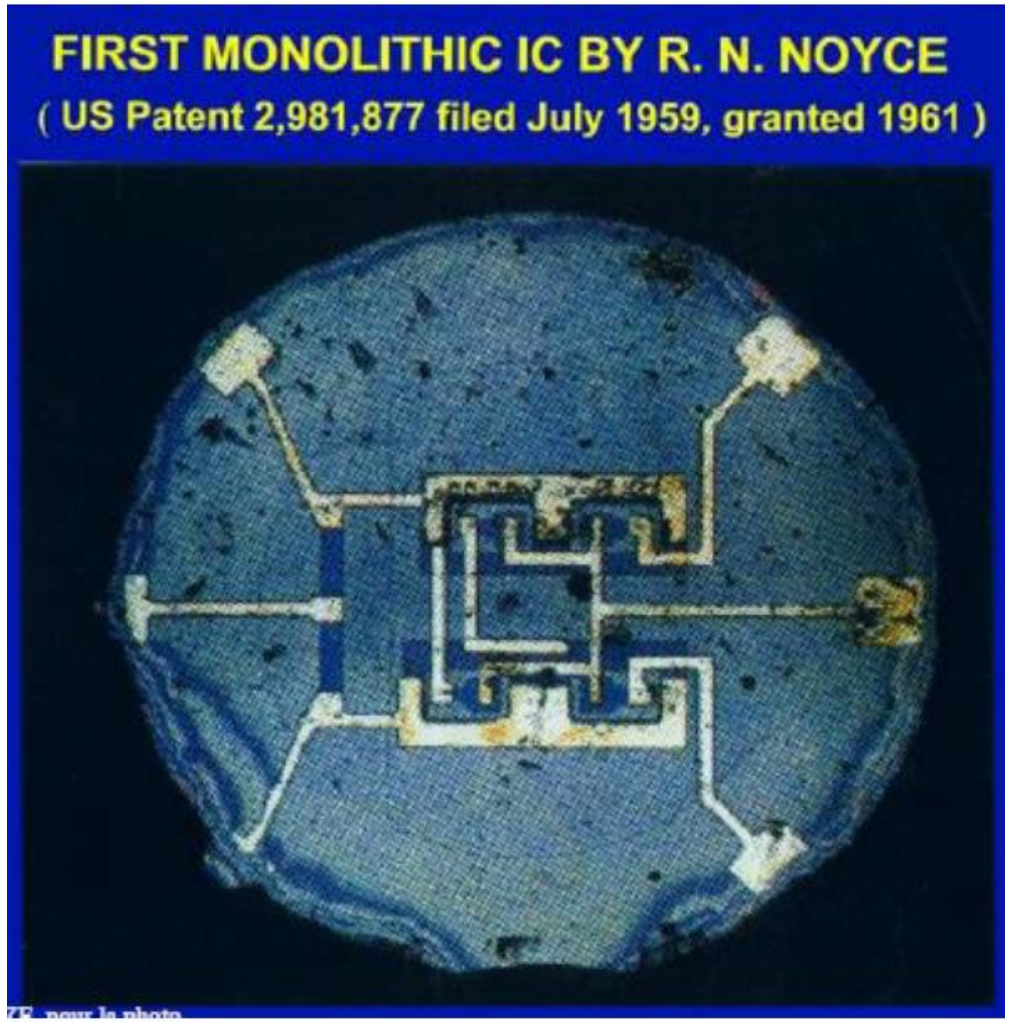
https://www.electronics-tutorials.ws/transistor/tran_7.html

From Integrated Circuit…

- **IC = a set of electronic circuits on one small flat piece (or "chip") of semiconductor (Si)**

- **The first monolithic IC was produced on May 26th 1960**

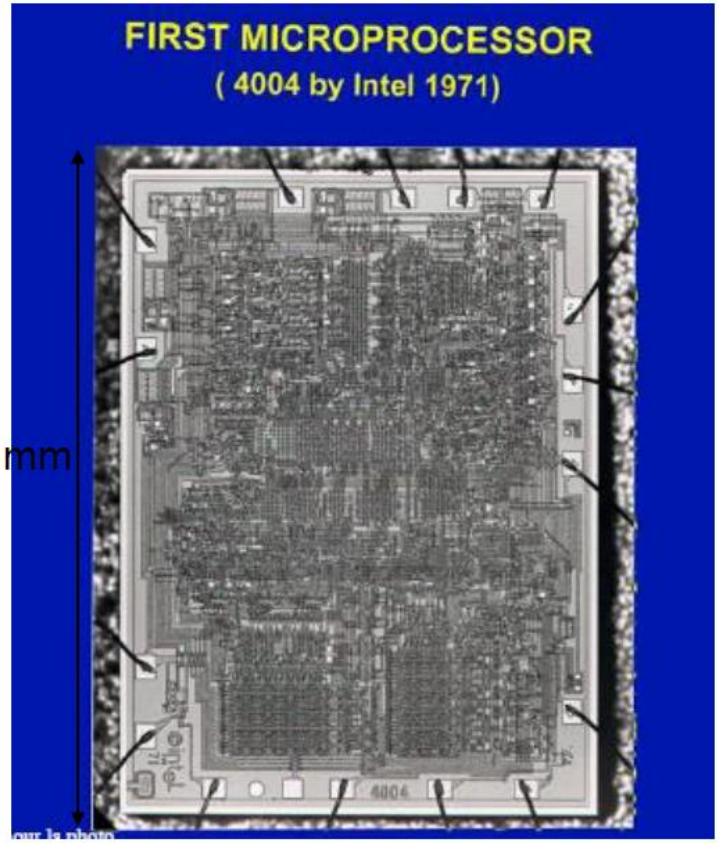
  → **Fabrication of all the components (transistors & resistances) on a same wafer by using oxide and Al contacts**

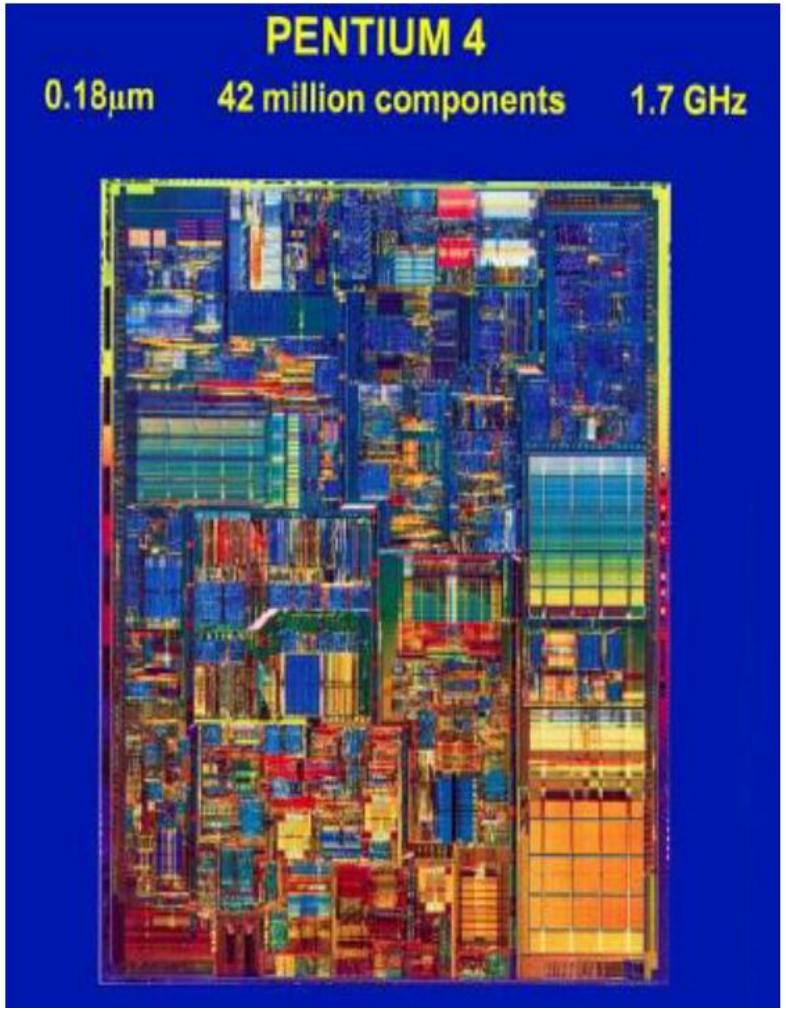


¼ of 2-inch

… to Microprocessor

- **First Microprocessor in 1971 (few thousands of MOS transistors)**
- **Pentium 4 in 2000 (42 millions of components)**



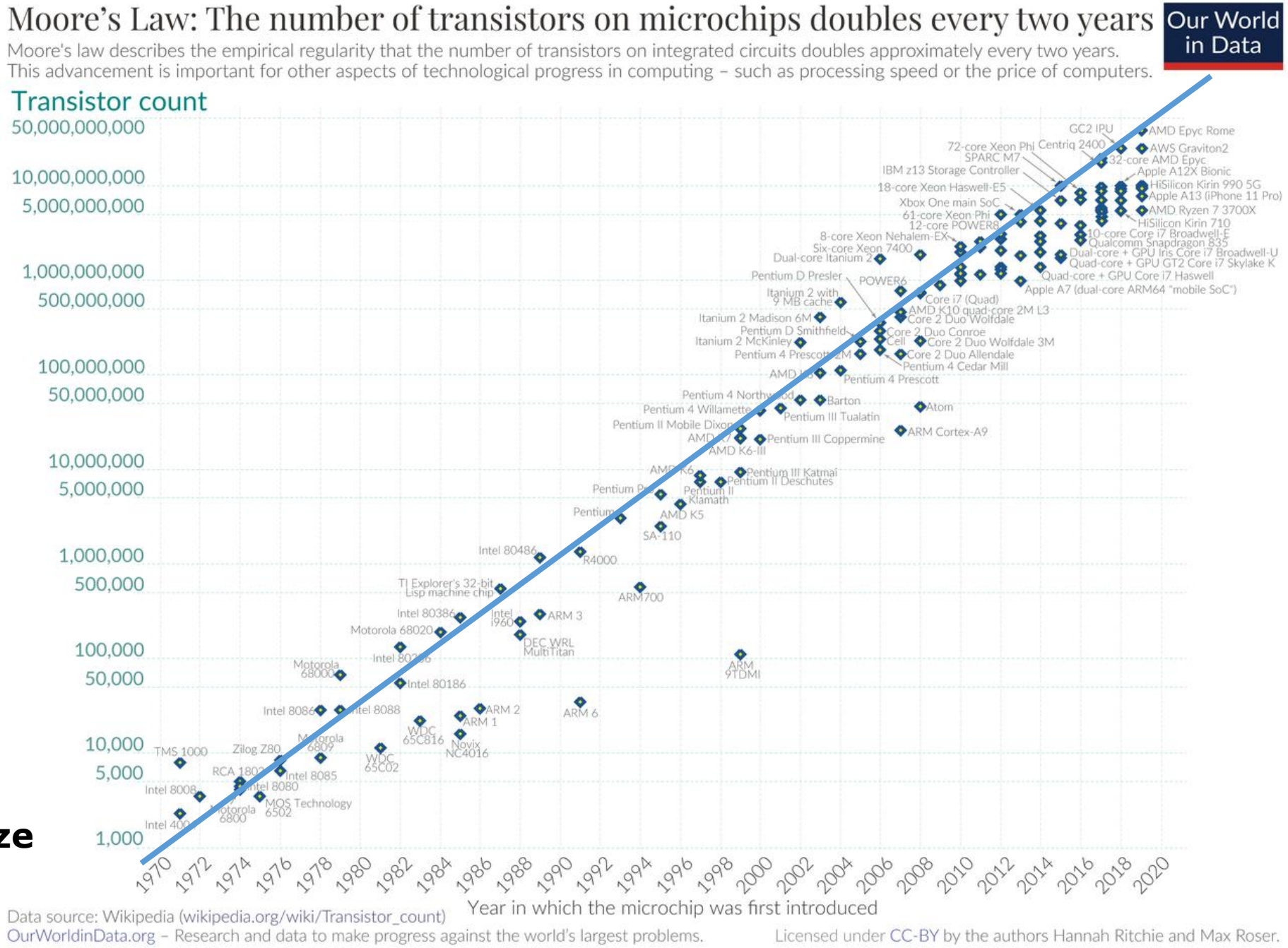


Moore’s Law

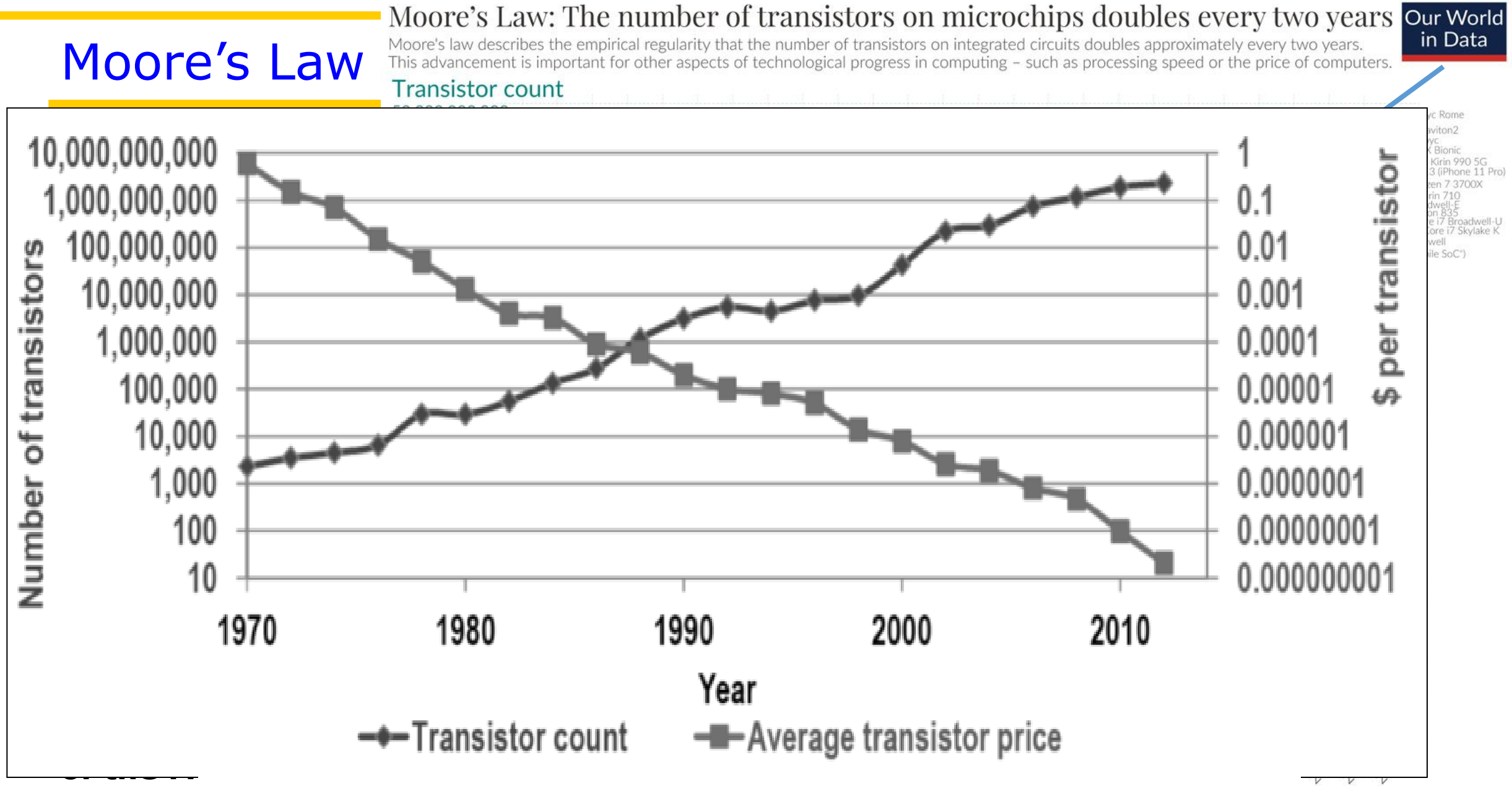
- **Moore’s Law:**

“Doubling in the number of components per integrated circuit (every 1.5 to 2-years)”
Gordon Moore (1965)

- **Reduction of the size of the MOSFET**



Moore's Law



➡ **The fabrication cost is divided by 10 every ~5 years**

Hannah Ritchie and Max Roser.

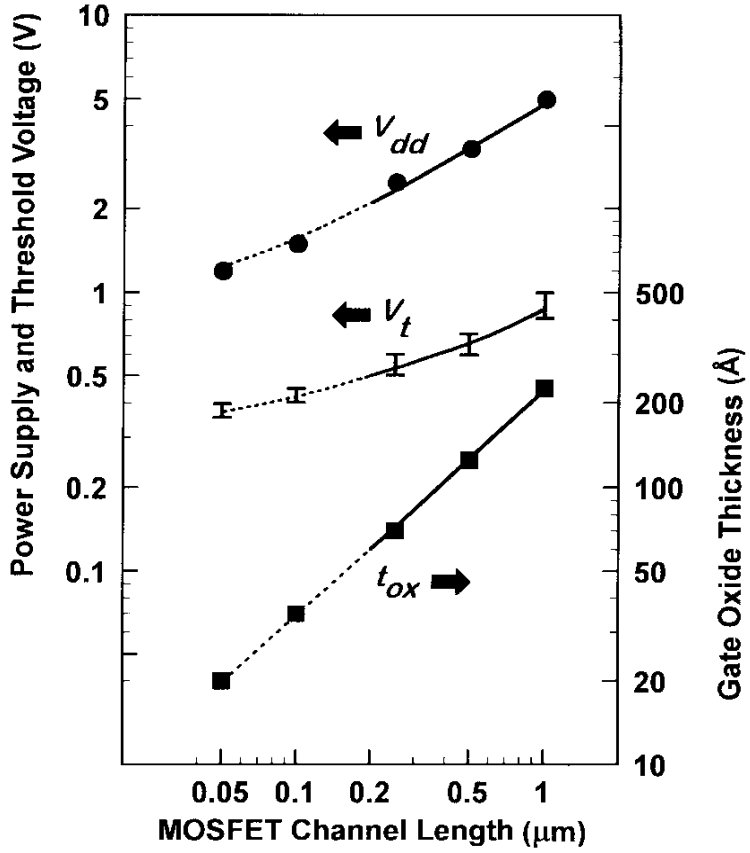
Transistor dimensions & performances

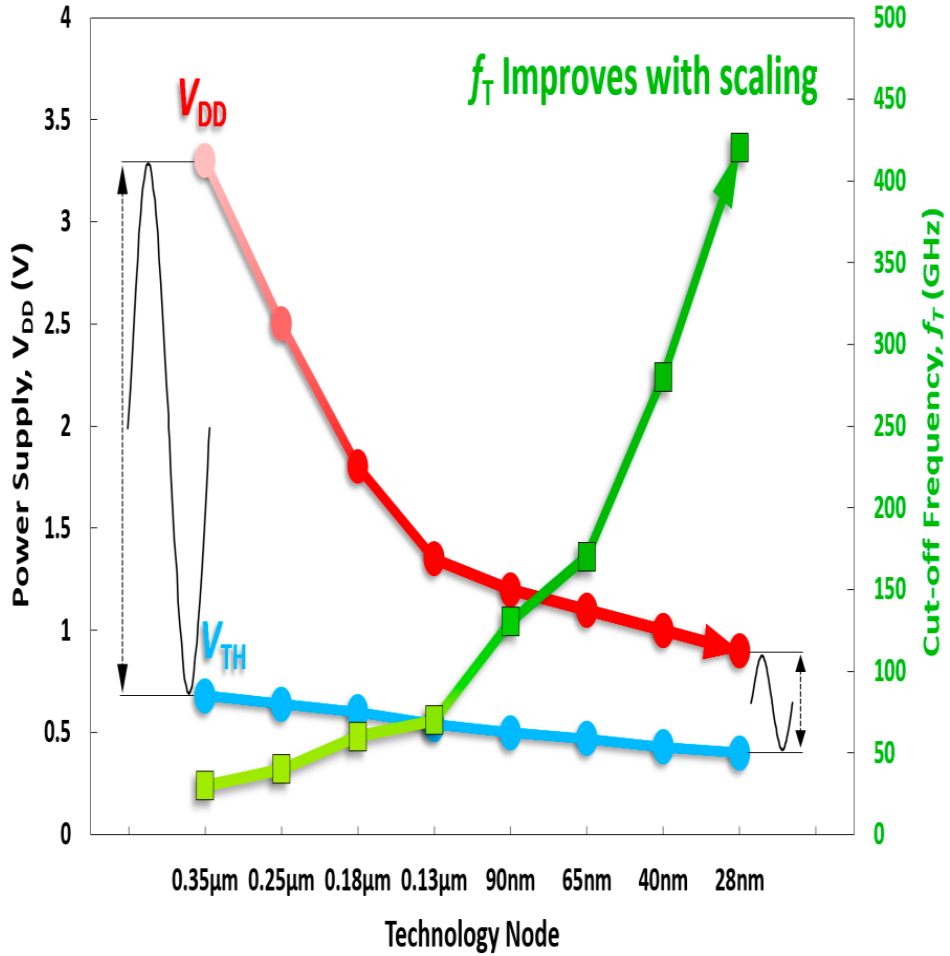
- **Following the scaling rules has a strong impact on the MOSFET performances**

V_{dd} : operating voltage

V_{th} (V_T): threshold voltage

t_{ox} : oxide thickness





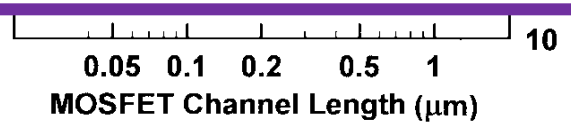
➡ **Increase of the maximum operating frequency**

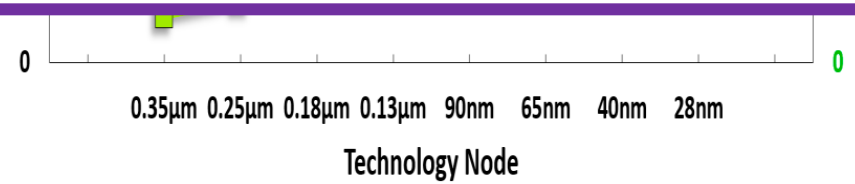
Transistor dimensions & performances

- **Following the scaling rules has a strong impact on the MOSFET performances**

Shrinking of the silicon transistors presents multiple benefits:

- **a lower power consumption,**
- **increased performance** (i.e. faster transistors operating at higher frequencies)
- **increasing functionality** (primary by increasing the transistor density)
- **a reduction in the fabrication cost per transistor…**





Transistor dimensions & performances

- **Following the scaling rules has a strong impact**

Proper scaling of MOSFET requires:

- a size reduction of the gate length and width **but NOT only**

--> it requires a reduction of all other dimensions

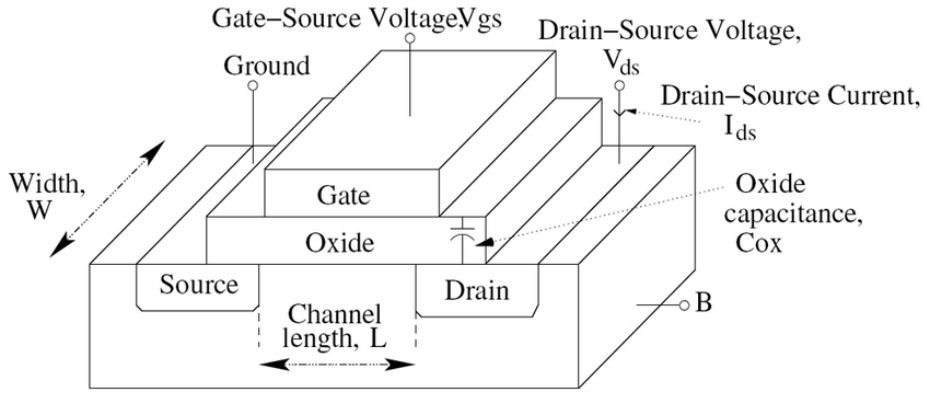
- **including the gate/source and gate/drain alignment,**
- **the oxide thickness and the depletion layer widths,**
- **scaling of the substrate doping density…**

Technology Node

Scaling rules

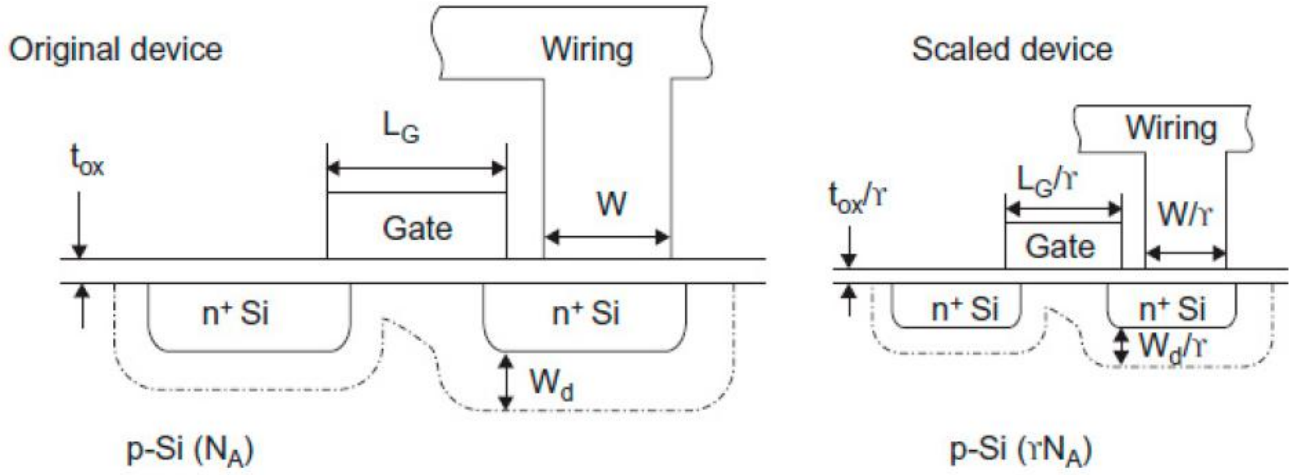
- **If a CMOS technology generation has:**
  - a minimum channel length and width (L & W),
  - an oxide thickness t_{ox},
  - a substrate doping N_A,
  - a power supply voltage V_{DD},
  - a threshold voltage V_{th}, etc.

- **Downscaling of the gate length and width, oxide thickness, junction depth, and substrate doping.**

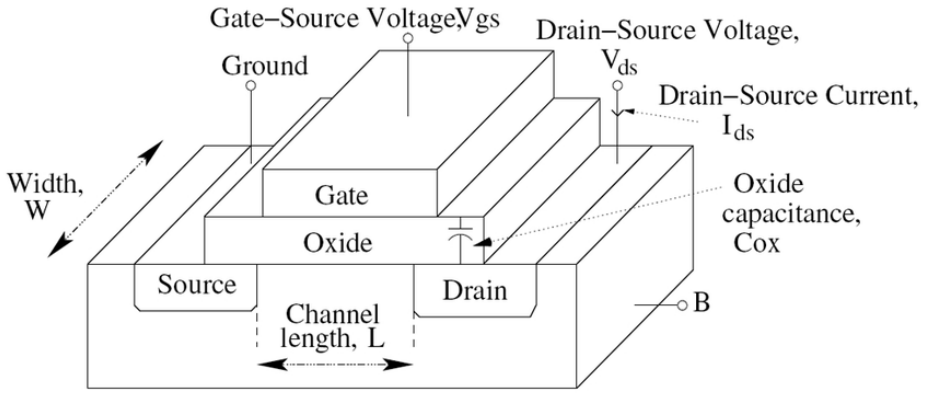


Supply and threshold voltages are also scaled by a factor of γ.

The electric field is constant
(rules developped by Robert Dennard in 1974).
The transistor density is increased by factor of γ^2.



Scaling rules

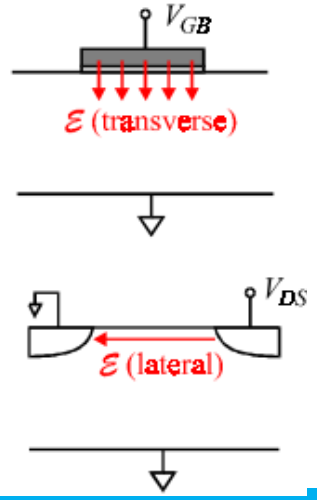


- **Two types of scaling (S = 1/0.7) can be used:**

1) constant voltage scaling

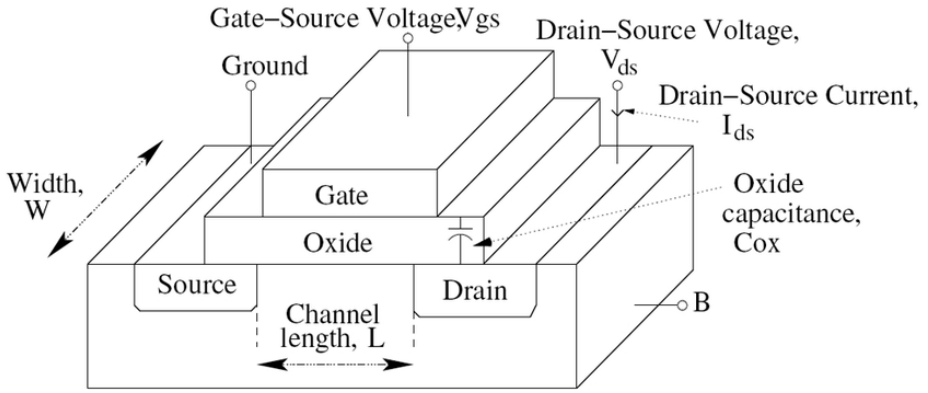
➡ **Avoid the previous problem = preferred scaling method since it provides voltage compatibility with older circuit technologies.**

The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages.



After Constant Voltage Scaling
$L' = L/s$
$W' = W/s$
$t'_{ox} = t_{ox}/s$
$x'_i = x_i/s$
$V'_{DD} = V_{DD}$
$V'_{Th} = V_{Th}$
$N'_a = N_a * s^2$ or $N'_d = N_d * s^2$
$C'_{ox} = C_{ox} * s$
$I'_{DS} = I_{DS} * s$
$P'_D = P_D * s$

Scaling rules



- **Two types of scaling (S = 1/0.7) can be used:**

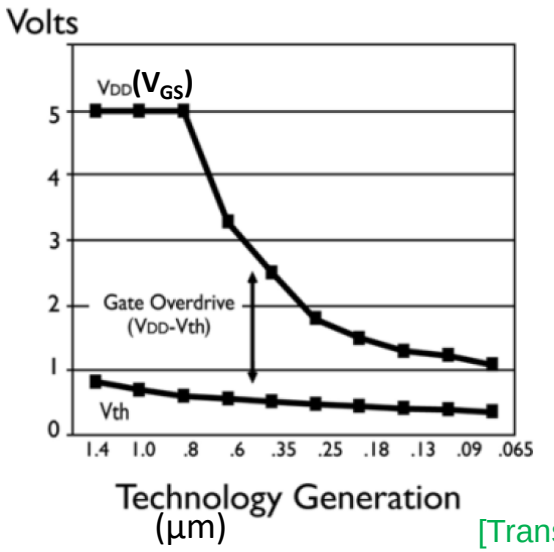
2) constant field scaling

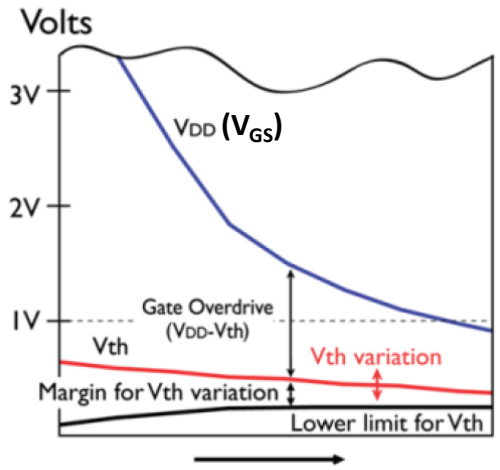
➡ **requires a reduction in V_{dd} as one decreases the minimum feature size.**

Difficulty of lowering V_{th}

Limit of MOSFET operation with a minimum overdrive voltage ($V_{DD} - V_{th}$)

Trade-off between performance & high-density leakage power dissipation





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$x'_i = x_i/s$
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$V'_{Th} = V_{Th}/s$
$N'_a = N_a * s$ or $N'_d = N_d * s$
$C'_{ox} = C_{ox} * s$
$I'_{DS} = I_{DS}/s$
$P'_D = P_D/s^2$

[Trans. Electr. Electron. Mater. 11(3) 93 (2010): Y.-B. Kim]

Fig. 1. Trend of supply voltage and threshold voltage scaling.

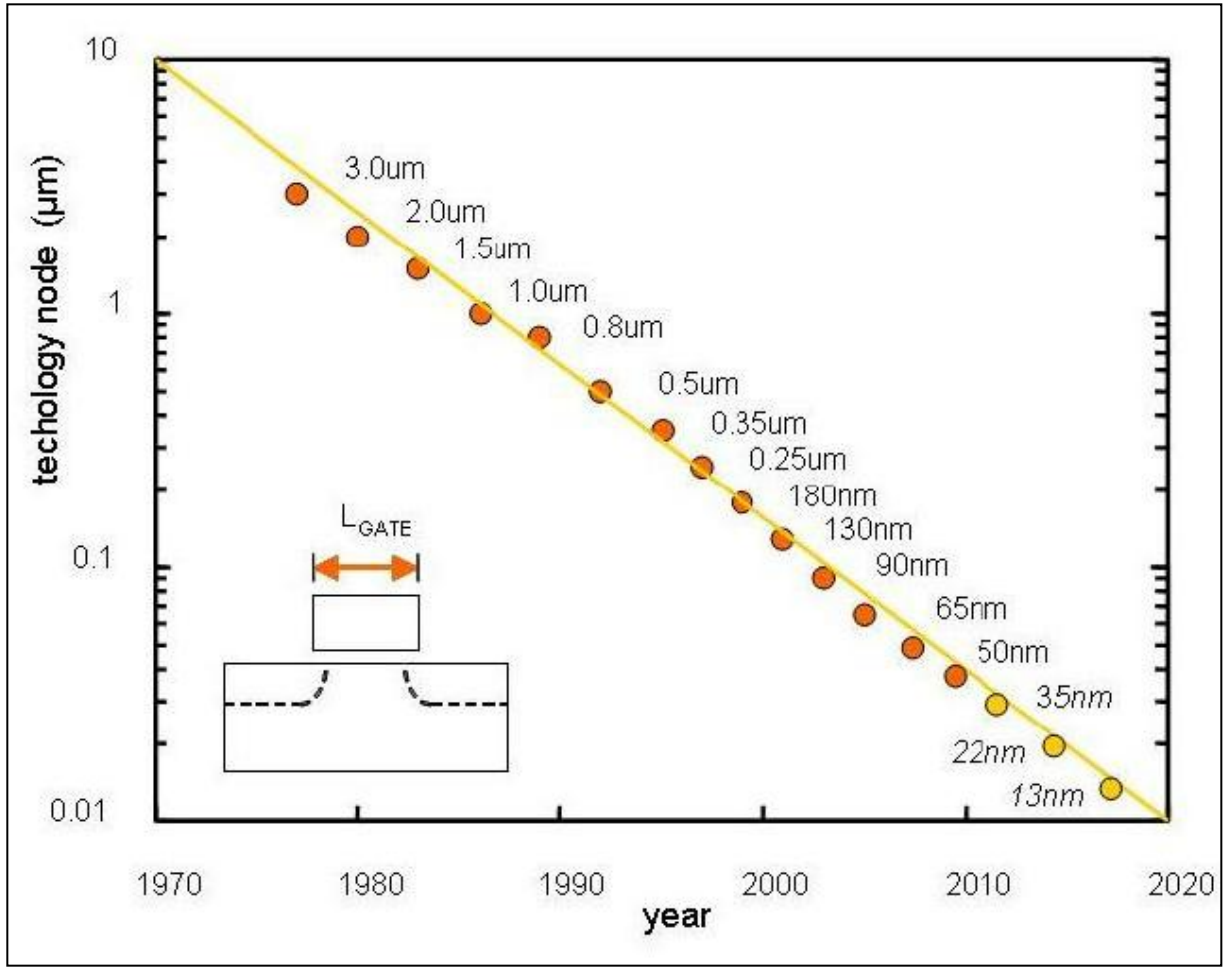
Limit in the Reduction of the transistor size

- **Evolution of the MOSFET transistor channel since 1970**

  Technology node (L_{gate})

- **As of 1980, the size reduction has been exponential**

- **Scaling to keep up with the demand for faster, smaller, cheaper products without any significant changes, relying on improved lithography processes** (used to transfer the electronics network patterns to every layer of IC)



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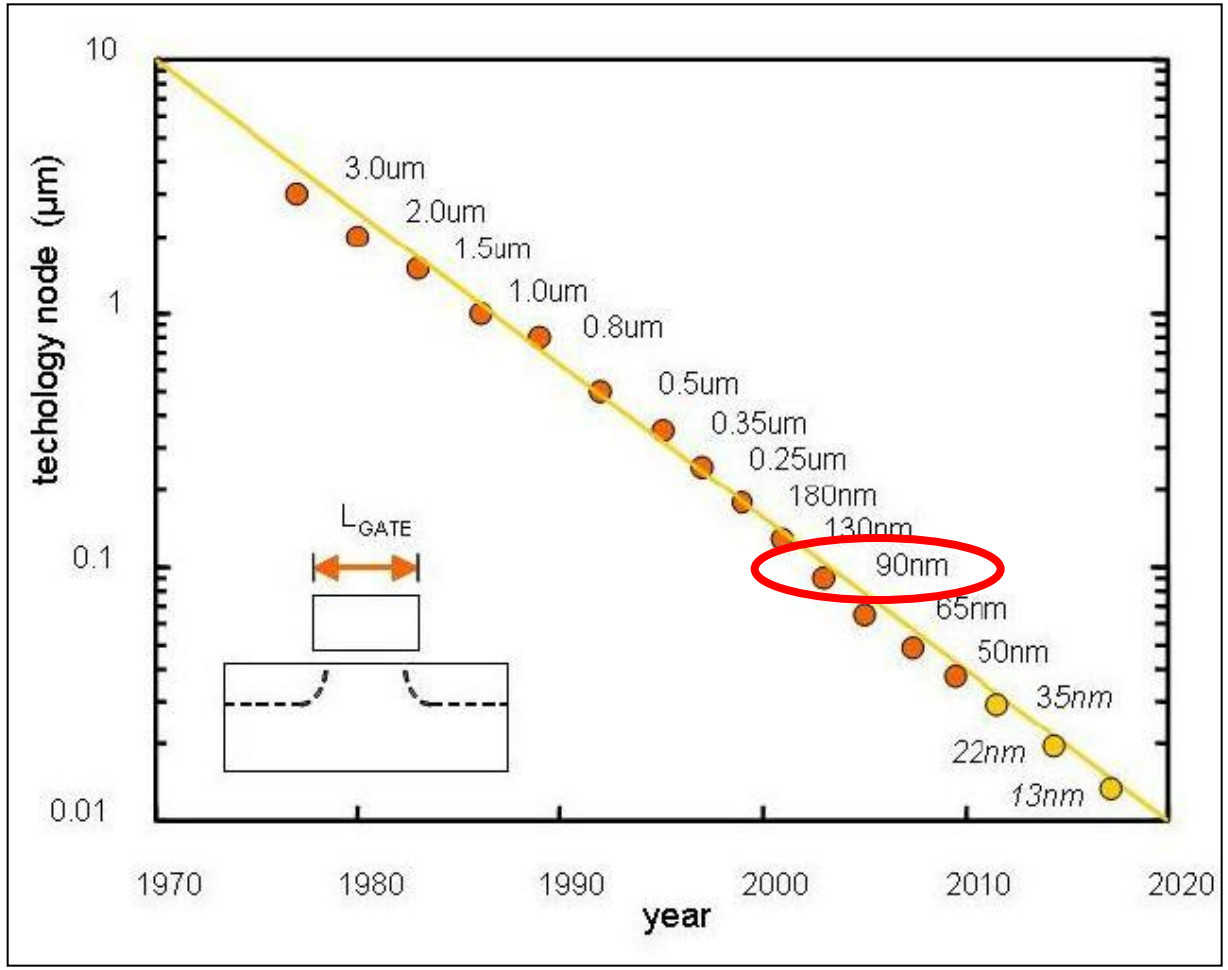
- **As the technology node reached 90 nm (in 2005), challenges started to appear !** ➡ **nano-electronic era**



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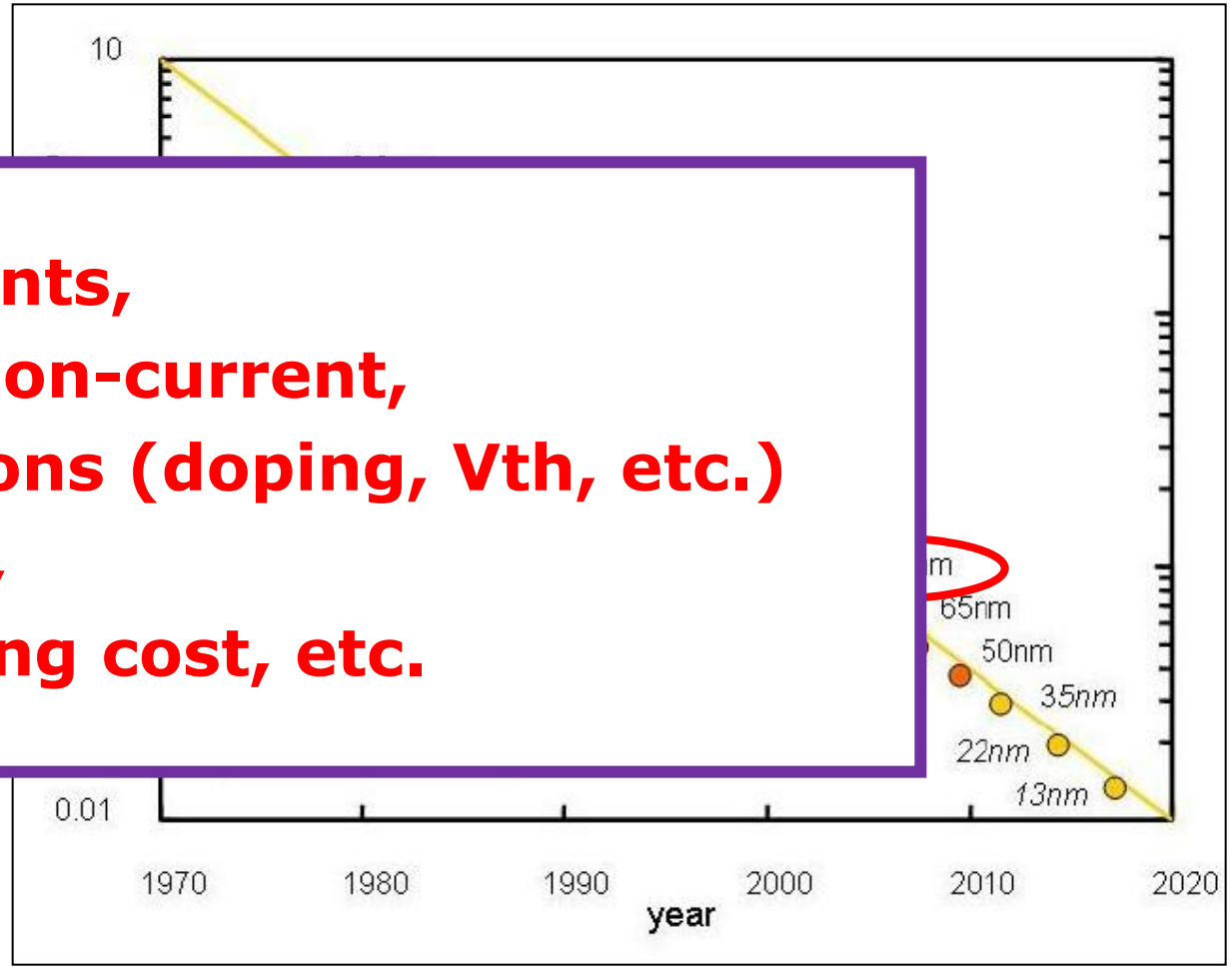
Techn

- **As of 19 has bee**

- **Scaling for faste without relying** (used to patterns

- **As the technology node reached 90 nm (in 2005), challenges started to appear !** ➡ **nano-electronic era**

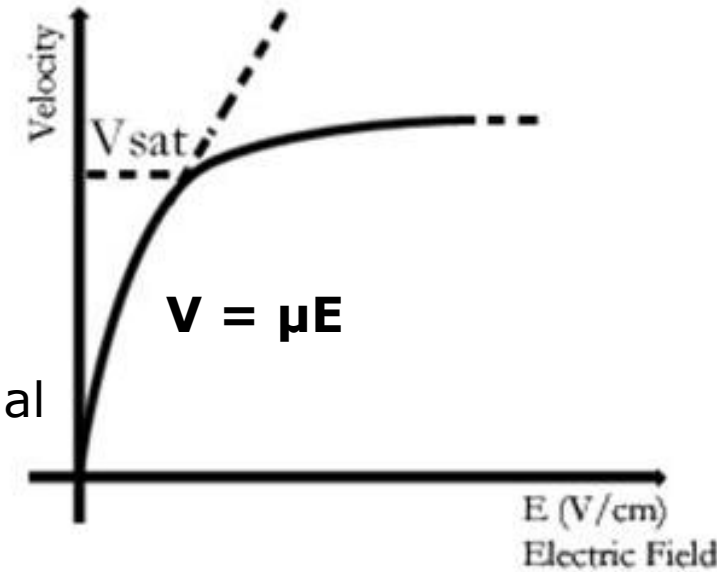
Increased leakage currents,
Difficulty on increase of on-current,
Large parameter variations (doping, Vth, etc.)
Low reliability and yield,
Increase in manufacturing cost, etc.

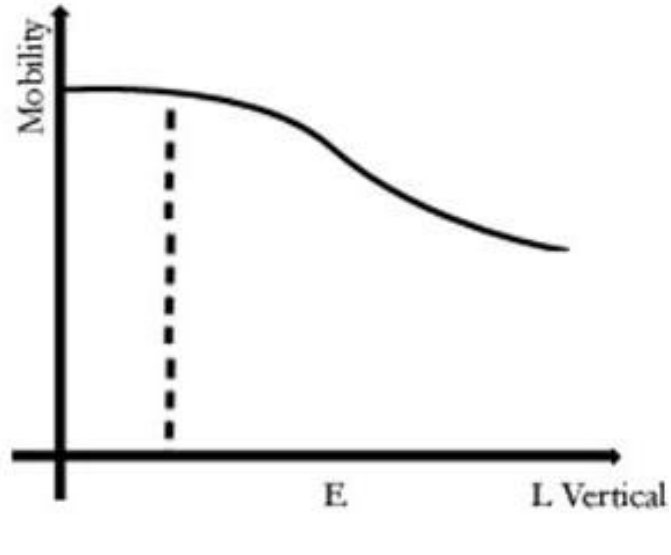


Velocity Saturation & Mobility Degradation

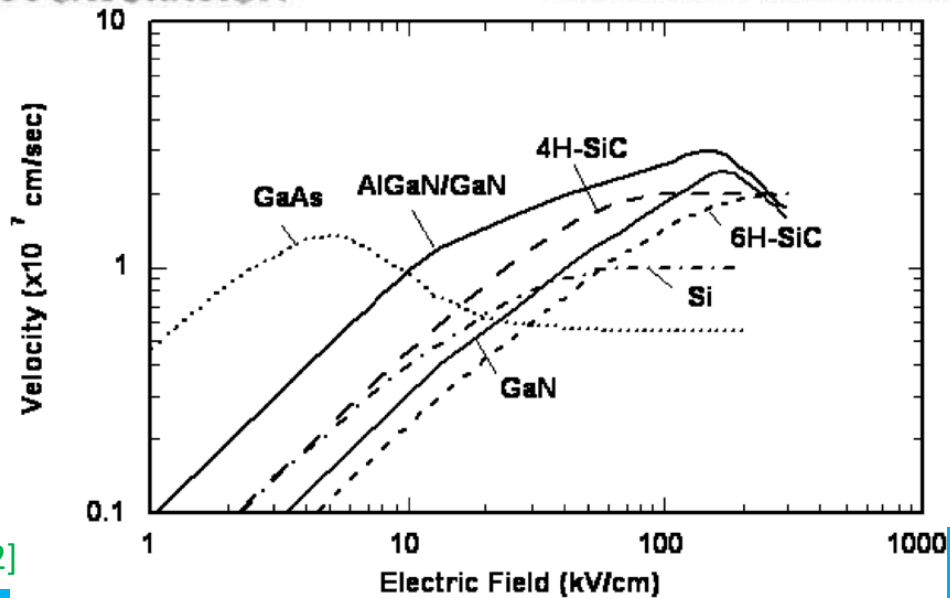
- The electron drift velocity in the channel is **proportional to the electric field @ low electric field values.**
- **It starts to saturate at high E.**
  ⟹ **velocity saturation (Vsat).**
- **For short channel devices**, the longitudinal electric field increases. At high E, **the velocity saturation affects the I-V characteristics of the MOSFET.**
- For the same V_{GS} (gate voltage), the saturation mode is reached at smaller values of V_{DS} and leads to saturation current reductions.
- Due to **higher vertical electric fields**, the carriers of the channel scatter off of the oxide interface.

  ⟹ **This results in the degradation of carrier mobility and the reduction in drain current.**





VELOCITY SATURATION MOBILITY DEGRADATION



[R. Trew, « High-Frequency Solid-State Electronic Devices », IEEE Trans. on Elec. Devices(2005), 10.1109/TED.2005.845862]

Velocity Saturation & Mobility Degradation

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- **It starts to**
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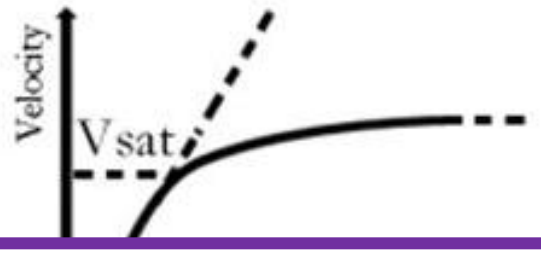
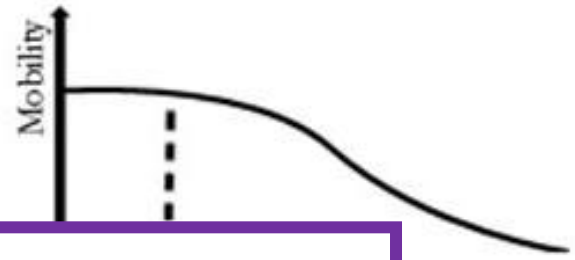
- Due to **high**, the carriers of the channel scatter off of the oxide interface.
  → **This results in the degradation of carrier mobility and the reduction in drain current.**





Both saturation field & the saturation velocity of a semiconductor material are typically strong function of:

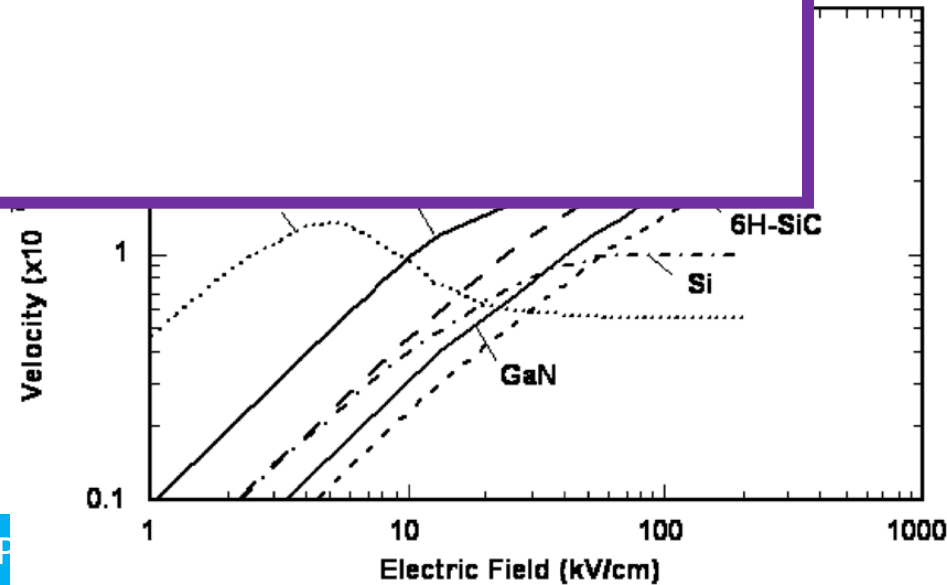
- impurities,

- crystal defects,

- operating temperature.

L Vertical

RADATION



IRDS nodes from 2020 to 2034

- **IRDS** (Int. Roadmap for Devices and Systems) **2020**

YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
	G48M36	G45M24	G42M20	G40M16	G38M16T2	G38M16T4
Logic industry "Node Range" labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	FinFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Mainstream device for logic	FinFET	FinFET	LGAA	LGAA	LGAA-3D	LGAA-3D
LOGIC TECHNOLOGY ANCHORS						
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Beyond CMOS as complimentary to mainstream CMOS	-	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat
Process, technology inflection	Conformal doping, Contact	Channel RMG	Lateral/ Atomic Etch	Non-Cu Mx	3D VLSI	3D VLSI
Stacking generation inflection	2D	3D stacking: W2W, D2W Mem-on-Logic	3D stacking: W2W, D2W Mem-on-Logic	3D stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic	3D stacking, 3D VLSI: Mem-on-Logic with Interconnect	3D stacking, 3D VLSI: Logic-on-Logic

Note: Mx—Tight-pitch routing metal interconnect. IDM—independent device manufacturer. FinFET—fin field-effect transistor. LGAA—lateral gate all around. EUV—extreme ultraviolet. NA—numerical aperture. Ge—germanium. SiGe—silicon germanium RMG—replacement metal gate. VLSI—very large scale integration. W2W—wafer to wafer. D2W—die to wafer. Mem-on-Logic—memory on logic

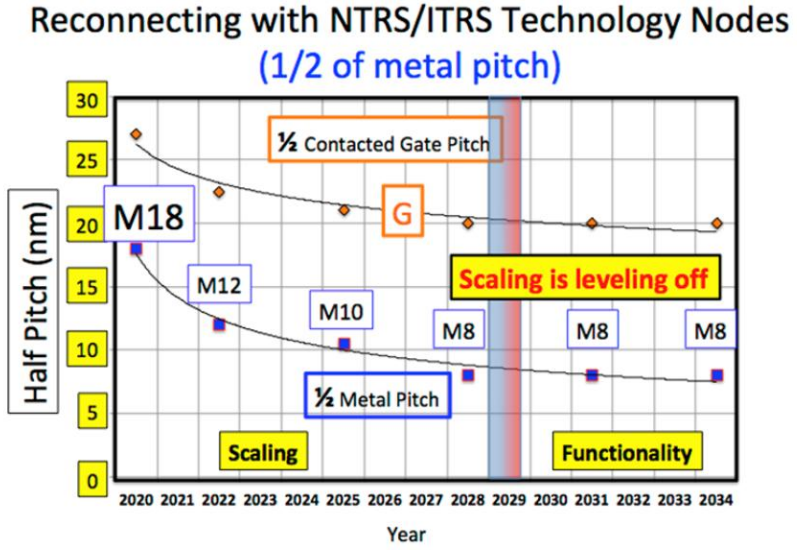
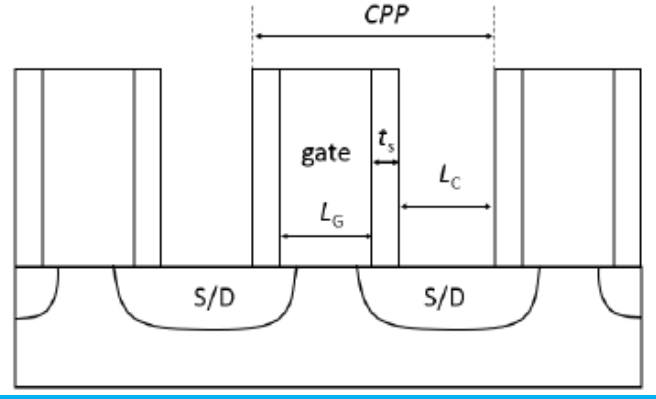


Figure ES31 Correct historical technology node definition and trend"

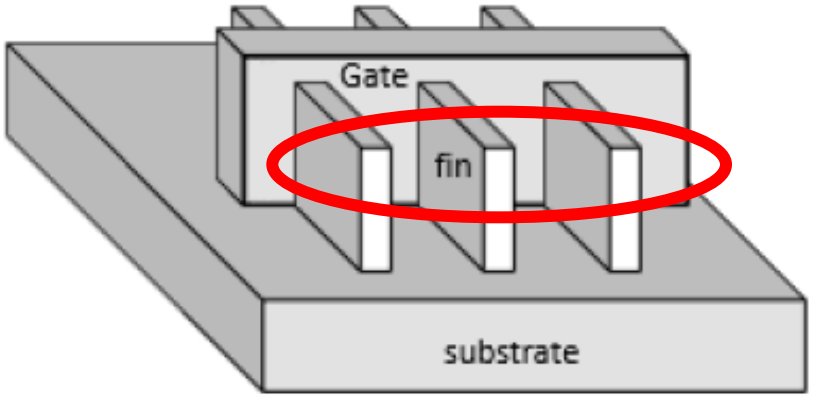
Figure ES31 shows also that feature scalin ecade. This prediction is consistent with forecasts of pected that quantum-computing technologies will beg ustry. (See Section 1.4.)



➡ **Modification/improvement of the device design**

FinFET Technology

- A fin field-effect transistor is a multi-gate device MOSFET built on a substrate where the gate is placed on 2, 3, or 4 sides of the channel or wrapped around the channel, forming **a double or even multi gate FET --> technology started to be implemented in 2011**

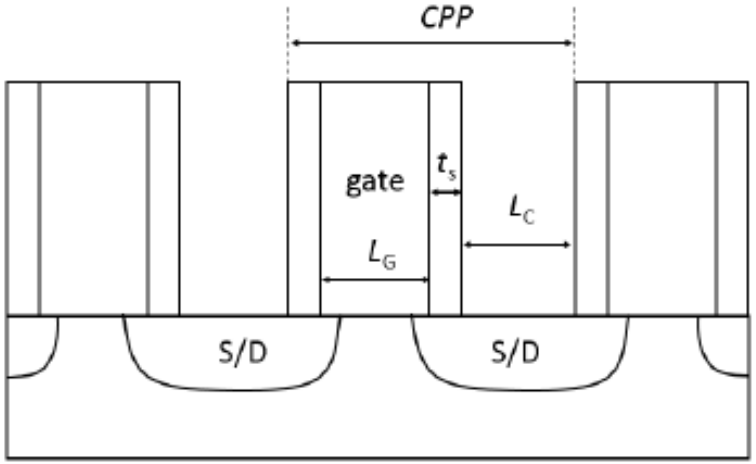


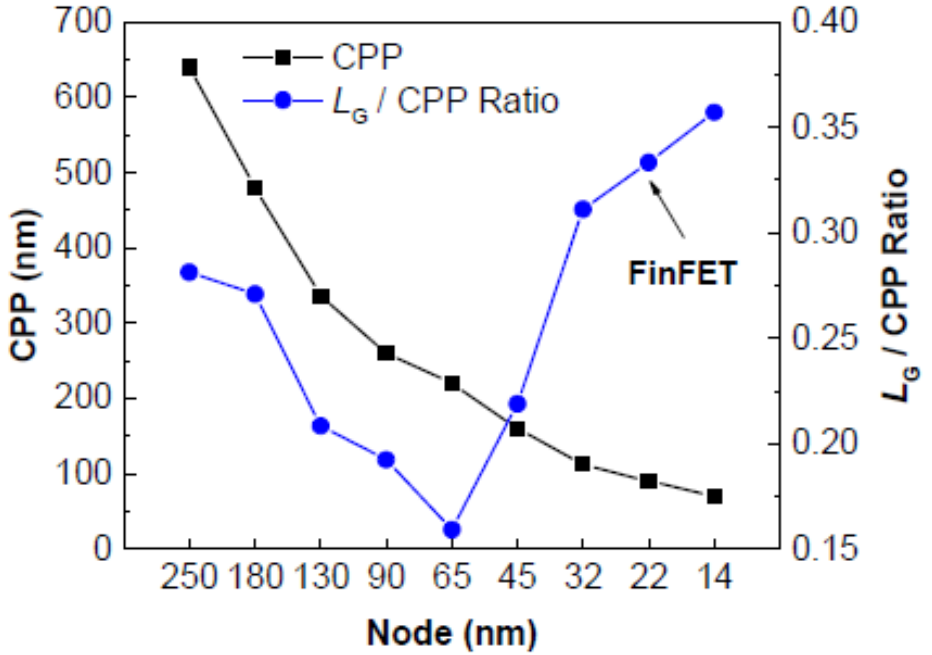
- **Excessive reduction of the gate length (L_G) in conventional MOSFET leads to an increase of the leakage current --> excessive stand-by power consumption.**
- **FinFET has improved electrostatics enabling the further scaling of L_G and contact gate/poly pitch (CPP).**

Reduction of V_{th}

- **active power consumption** (reduction of V_{DD})
- **performances** (@cst $P_{consumption}$)

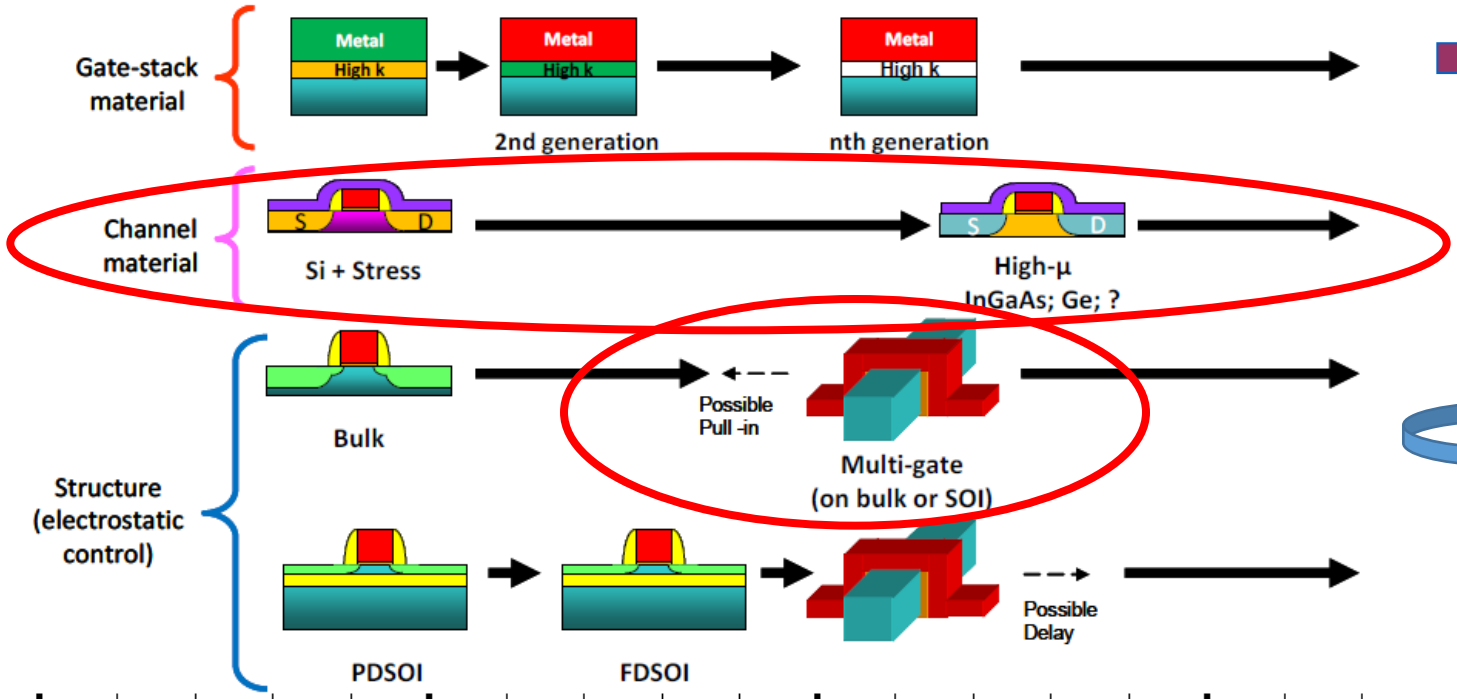
[K. Cheng et al., ECS Transactions 80, 17 (2017)]





Improvement of the Performances

- **ITRS** (Int. Tech. Roadmap for Semicond.) **2010**



2009 ITWG Table Timing:	2007		2010		2013		2016		2019	2021
2009 IS ITRS Flash Poly :	54nm	45nm	2009	32nm	2012	22nm	2015	16nm	2018	11nm	2021
2009 IS ITRS DRAM M1 :	68nm			45nm		32nm		22nm		16nm	
MPU/hpASIC "Node":	"45nm"		"32nm"		"22nm"		"16nm"		"11nm"	"8nm"	
2009 ITRS MPU/hpASIC M1 :	76nm	65nm	54nm	45nm	38nm	32nm	27nm		19nm	13nm	
2009 ITRS hi-perf GLpr :	54nm	47nm	47nm	41nm	35nm	31nm	28nm		20nm	14nm	
2009 ITRS hi-perf GLph :	32nm	29nm	29nm	27nm	24nm	22nm	20nm		15nm	12nm	

(Dashed arrows indicate additional timing movement considerations for 2011 ITRS work.)

Heterogeneous integration

- **High mobility materials (SiGe, III-V)**

introduction on a Si platform and a multi-gate based technology

--> Compatibility with the FinFET-based technology

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Stacking generation inflection	2D	3D stacking: W2W, D2W Mem-on-Logic	3D stacking: W2W, D2W Mem-on-Logic	3D stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic	3D stacking, 3D VLSI: Mem-on-Logic with Interconnect	3D stacking, 3D VLSI: Logic-on-Logic

Note: Mx—Tight-pitch routing metal interconnect. IDM—independent device manufacturer. FinFET—fin field-effect transistor. LGAA—lateral gate all around. EUV—extreme ultraviolet. NA—numerical aperture. Ge—germanium. SiGe—silicon germanium. RMG—replacement metal gate. VLSI—very large scale integration. W2W—wafer to wafer. D2W—die to wafer. Mem-on-Logic—memory on logic

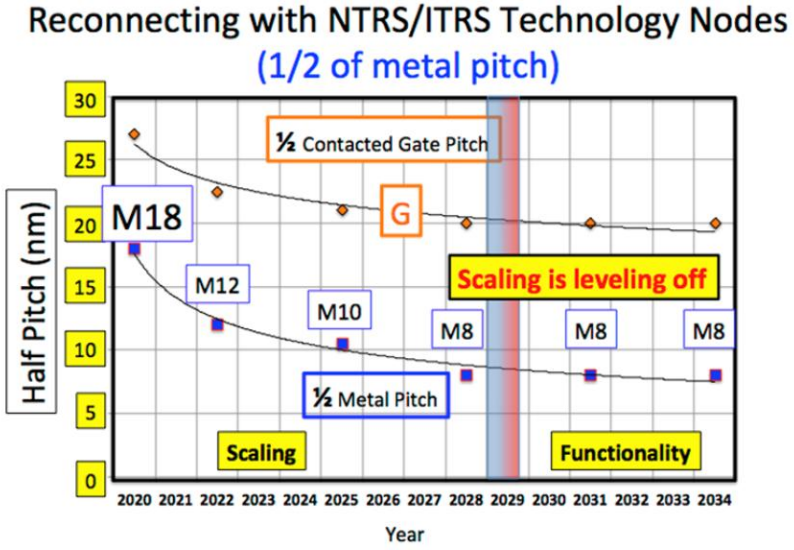
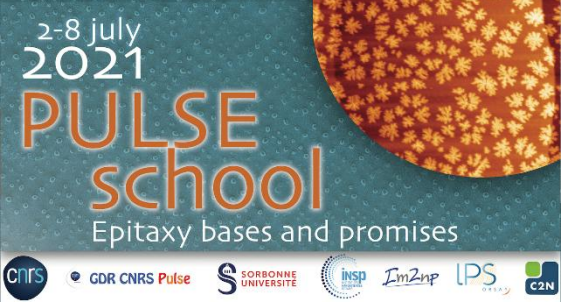


Figure ES31 Correct historical technology node definition and trend"

Figure ES31 shows also that feature scaling will reach fundamental limits of around 7-8 nm at the end of this decade. This prediction is consistent with forecasts of equipment technology leaders.[4] However, by early 2030 it is expected that quantum-computing technologies will begin to make real contributions to the advancement of the electronics industry. (See Section 1.4.)

➡ **Modification/improvement of the channel structure**

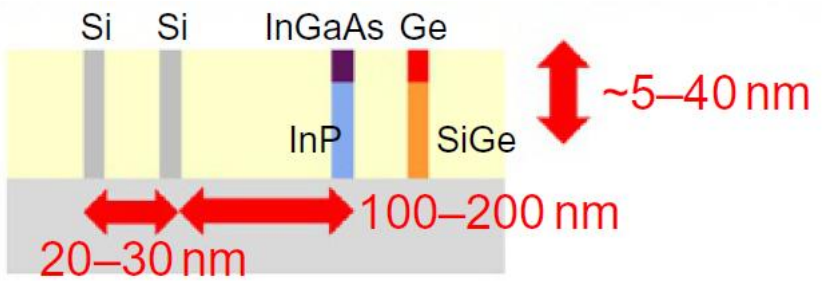


Heterogeneous Integration

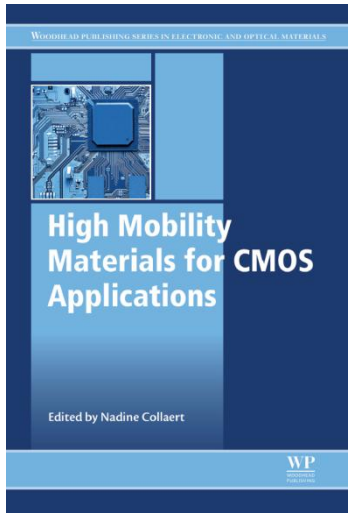
Heterogeneous Material Integration on Si Platforms

- **Growing need to integrate more functionality into a smaller form factor with power-performance benefits**
- **Need for disruptive solutions to solve Si CMOS scaling limitations**
  → **new on-chip functionalities** (sensors, optoelectronics, power management, RF…)
- **Complex electronic system are still fabricated using a wide range (mix) of technologies** (combining chips of last generation CMOS with older process technology chips in RF, MEMS…)
- **Integration of heterogeneous components for performance, power & cost improvement**
  → **Beyond multichip modules & system in package**

  ↻ **on-chip integration**



→ **Co-integration at the material level**
(in a compact volume)



High Mobility Materials for CMOS Applications.
https://doi.org/10.1016/B978-0-08-102061-6.00001-X

Heterogeneous Material Integration on Si Platforms

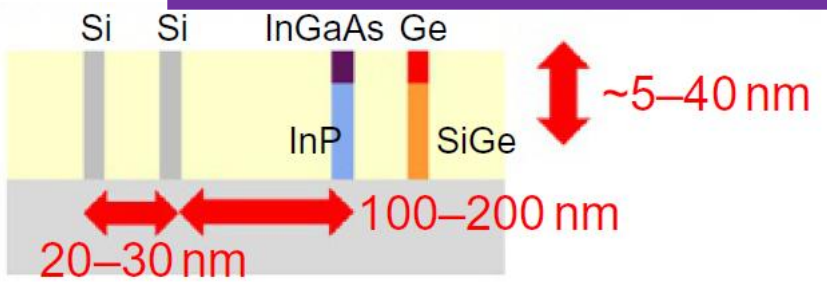
- **Growing need to integrate more functionality into a smaller form factor with power-performance benefits**
- **Nee**
- **Cor** (Mix
- **Pre imp**

Compatibility with large-scale 300 mm CMOS processes

Epitaxial techniques/processes adapted to:

- **Defect**
- **Stress**
- **Thermal budget**

} **management**



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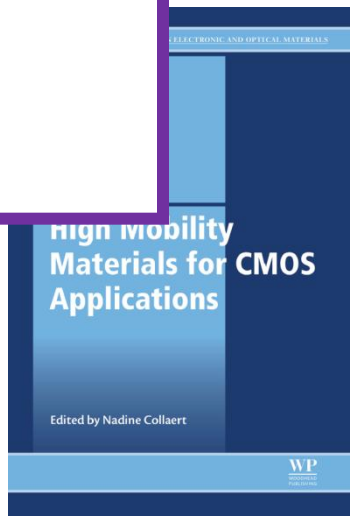

High Mobility Materials for CMOS Applications.
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Heterogeneous Material Integration on Si Platforms

- **Integrate** (onto Si) **heterogeneous devices with CMOS transistors**
  → **introduction of materials with specific properties**

- **Semiconductor materials chosen for their specific properties (E_g, μ)**

  e.g. InP, InGaAs, GaAs and GaN developed for mixed-signal analog RF applications

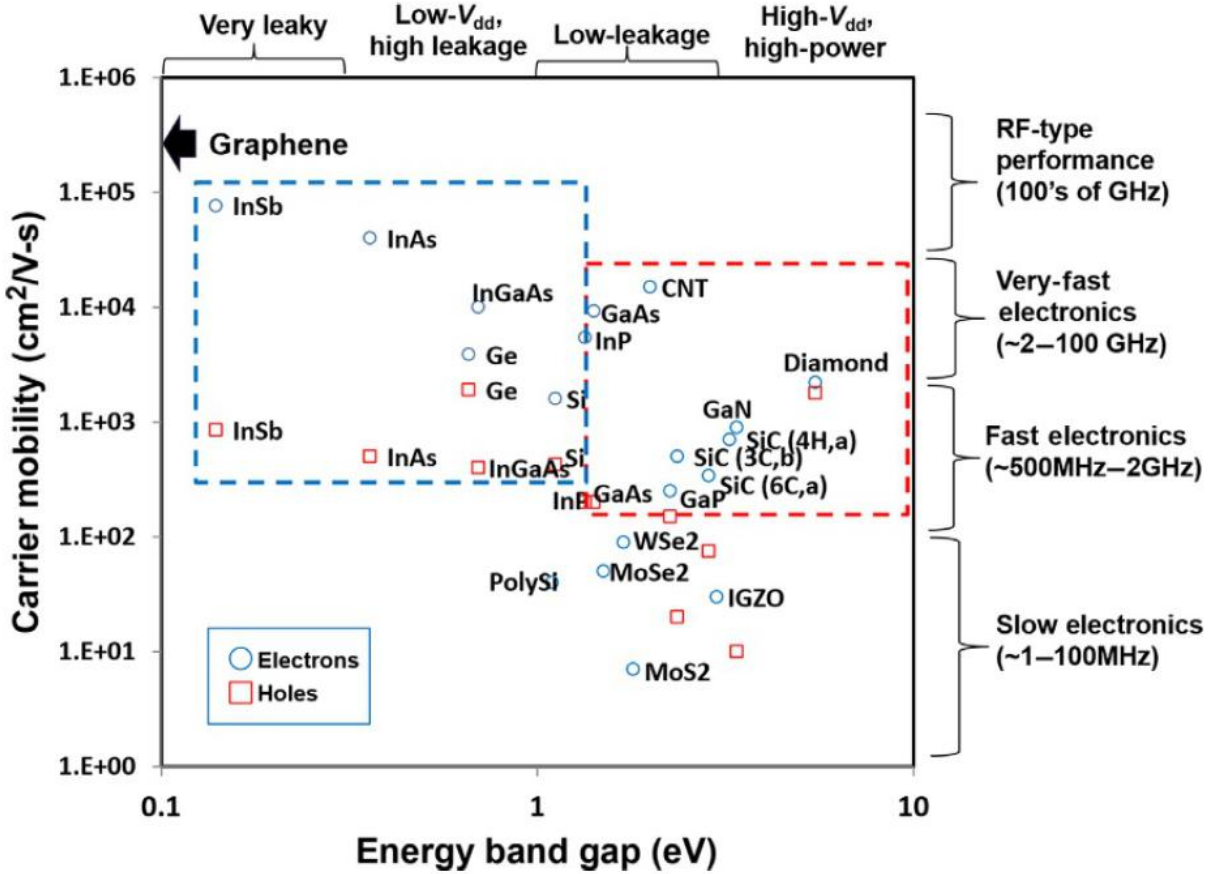

FIG. 2.8 Comparison of electron/hole carrier mobilities and energy bandgaps of selected semiconductors. *Red* box: these are some materials capable of low-leakage and high-voltage operations with switching speeds suitable for fast electronics. *Blue* box: lower bandgap materials with potential for significantly faster than silicon switching, low-voltage operations, and wide-spectrum optoelectronic response.

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- **Integrate** (onto Si) **heterogeneous devices with CMOS transistors**
  → **introduction of materials with specific properties**

- **Semiconductor materials chosen for their specific properties (E_g, μ)**

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Replacement of the Si channel of the MOSFET

- **Use of strained Si**
- **Use of SiGe technology**
- **Use of a III-V material**

} **characterized by a higher mobility**

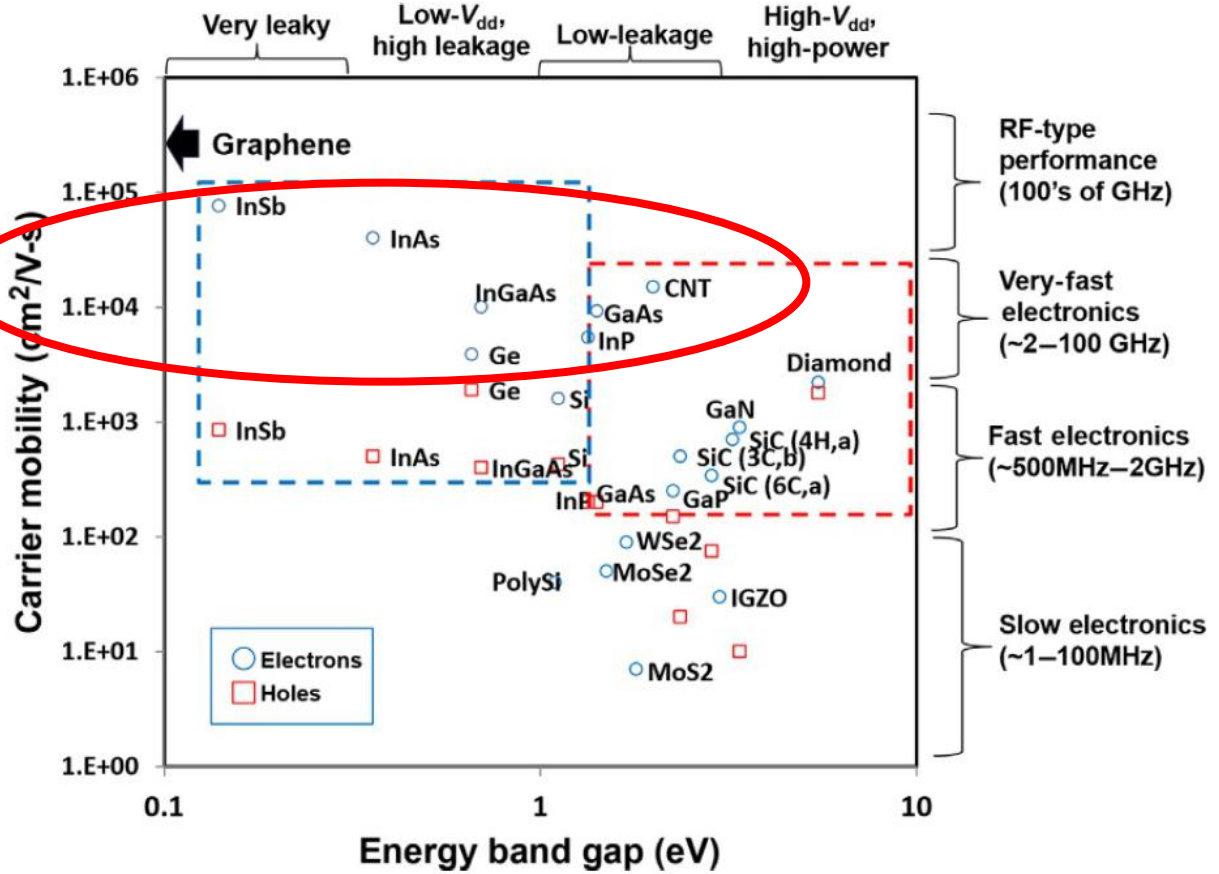


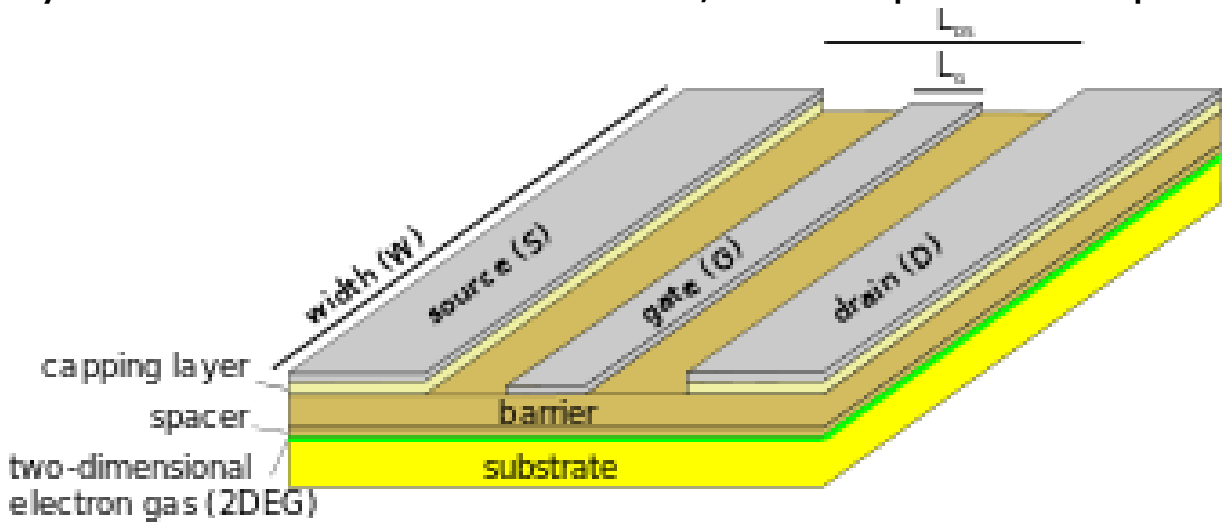
FIG. 2.8 Comparison of electron/hole carrier mobilities and energy bandgaps of selected semiconductors. *Red* box: these are some materials capable of low-leakage and high-voltage operations with switching speeds suitable for fast electronics. *Blue* box: lower bandgap materials with potential for significantly faster than silicon switching, low-voltage operations, and wide-spectrum optoelectronic response.

High Electron Mobility Transistor

- **A high-electron-mobility transistor (HEMT)** is a FET incorporating a **heterojunction between two materials with different band gaps as the channel instead of a doped region** (as is generally the case for a MOSFET)**.**

- **HEMTs are used in integrated circuits as digital on-off switches & as amplifiers.** They are able to operate at higher frequencies than ordinary transistors, up to millimeter wave frequencies.

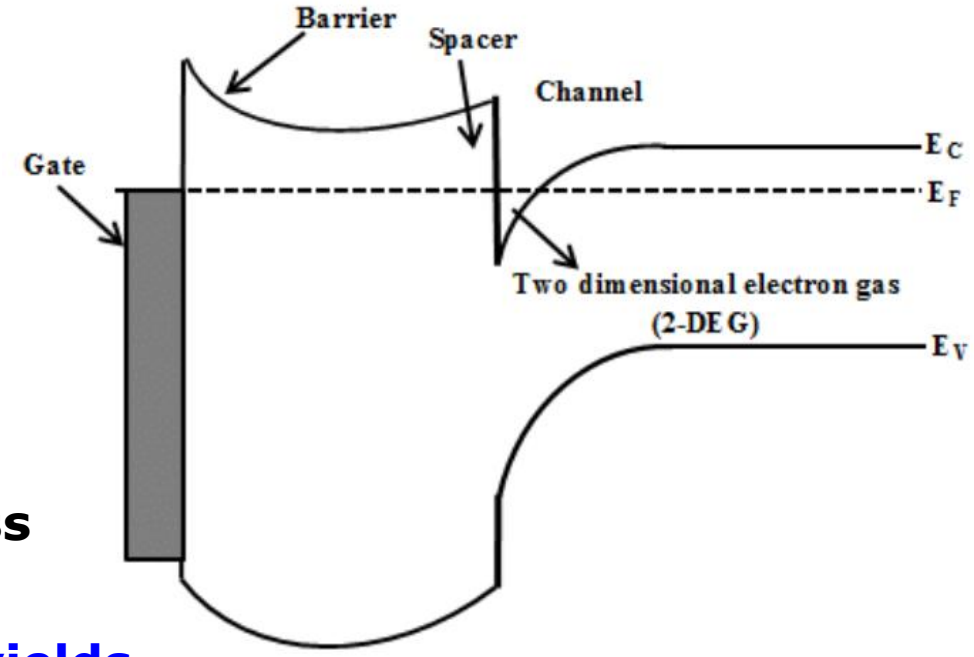
- **Applications: high-frequency products** such as cell phones, satellite television receivers, voltage converters, and radar equipment. They are widely used in satellite receivers, in low power amplifiers and in the defense industry.



https://en.wikipedia.org/wiki/High-electron-mobility_transistor

High Electron Mobility Transistor

- **The HEMT high carrier mobility and switching speed come from his specific design:**
- The wide band element (barrier) is typically doped with donor atoms and has excess electrons in its conduction band.
  The e- diffuse to the adjacent narrow band material CB due to the availability of states with lower energy.
  The movement of electrons will cause a change in potential and thus an electric field between the materials.
  The electric field will push electrons back to the wide band element CB. The diffusion process continues until electron diffusion and electron drift balance each other, creating a junction at equilibrium similar to a p-n junction.
  The undoped narrow band gap material now has excess majority charge carriers --> 2DEG



Supriya, Sweety. (2012).
Ballistic Mobility Degradation Effect in 25 nm Single Gate HEMT.

The fact that the charge carriers are majority carriers yields high switching speeds, and the fact that the low band gap semiconductor is undoped means that there are no donor atoms to cause scattering and thus yields high mobility.

Band Structure Engineering

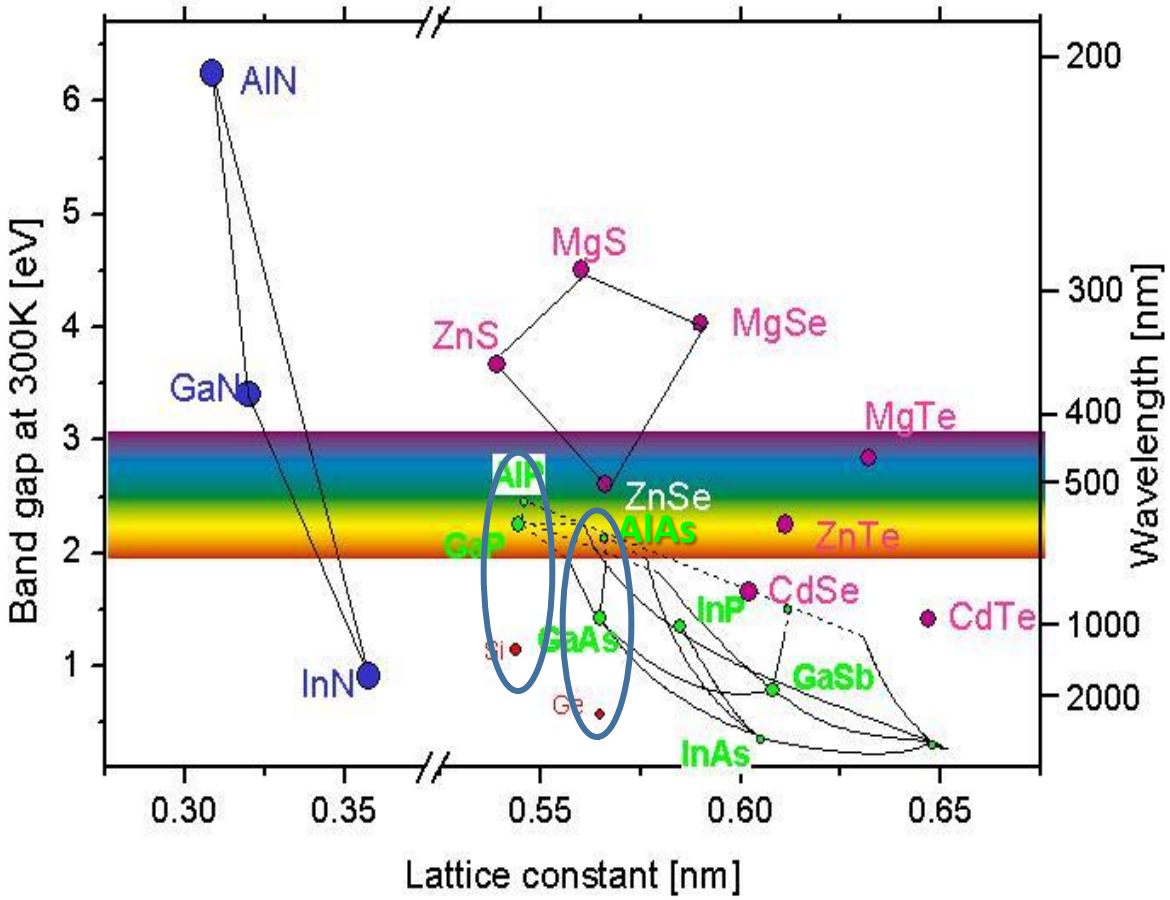
- **Heteroepitaxy → band structure design & engineering for high performance devices**

- **Combining different III-V materials leads to a large variety of band structures (band alignments)**

  → **Fabrication of complex heterostructures**

  In lattice-matched systems:
  - Si, GaP, AlP
  - Ge, GaAs, AlAs

  Using III-V alloys:
  - (In,Ga,Al)As
  - (In,Ga,Al)P
  - (In,Al,Ga)N



Band Structure Engineering

- **Heteroepitaxy → band structure design & engineering for high performance devices**

- **Epitaxial stress:**
  $\varepsilon = (a_{sub.} - a_{lay.}) / a_{lay.}$

  → **$\varepsilon < 0$: compressive stress**
  $\varepsilon > 0$: tensile stress

  ↺ **Critical thickness**
  (pseudomorphic growth)

  $h_c \propto 1 / \varepsilon$

  For $h > h_c$: strain relaxation
  (creation of defects)

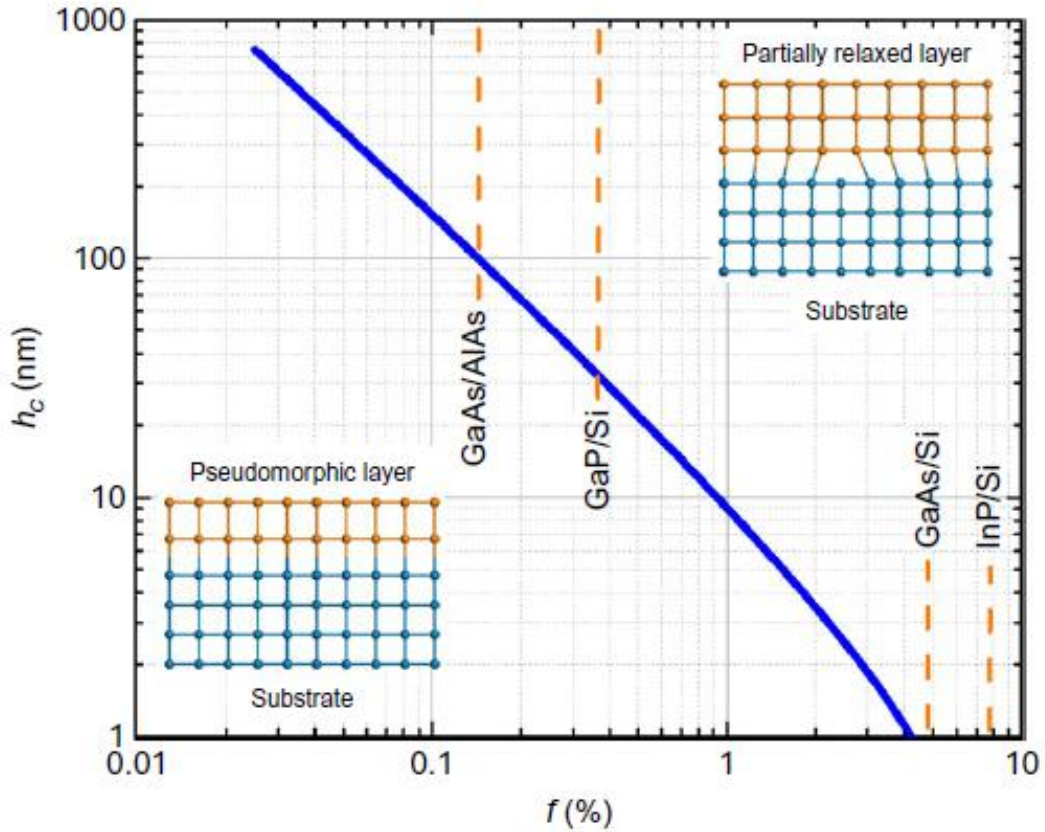
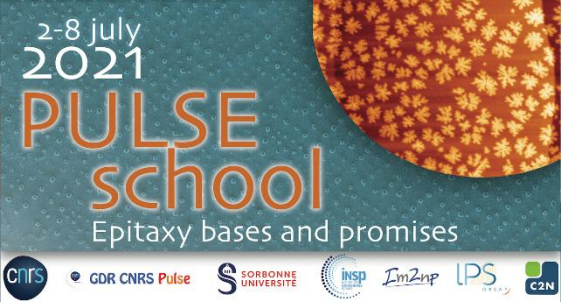


FIG. 3.3 Theoretical critical thickness h_c in function of lattice mismatch f.

Chapter 3 – Monolithic Integration of InGaAs on Si(001) Substrate for Logic Devices , Clément Merckling
High Mobility Materials for CMOS Applications. https://doi.org/10.1016/B978-0-08-102061-6.00004-5



Epitaxy Defect Engineering

Heterogeneous Material Integration on Si Platforms

- **Key challenge --> elimination of the dislocations formed when Ge or III-V materials are grown on Si.**
  - **A variety of techniques includes:**
    - **compositional grading,**
    - **wafer bonding,**
    - **selective area growth,**
    - **aspect ratio trapping,**
    - **cyclic annealing.**

[D. Caimi et al., Solid-State Electronics 185, 108077 (2021)]

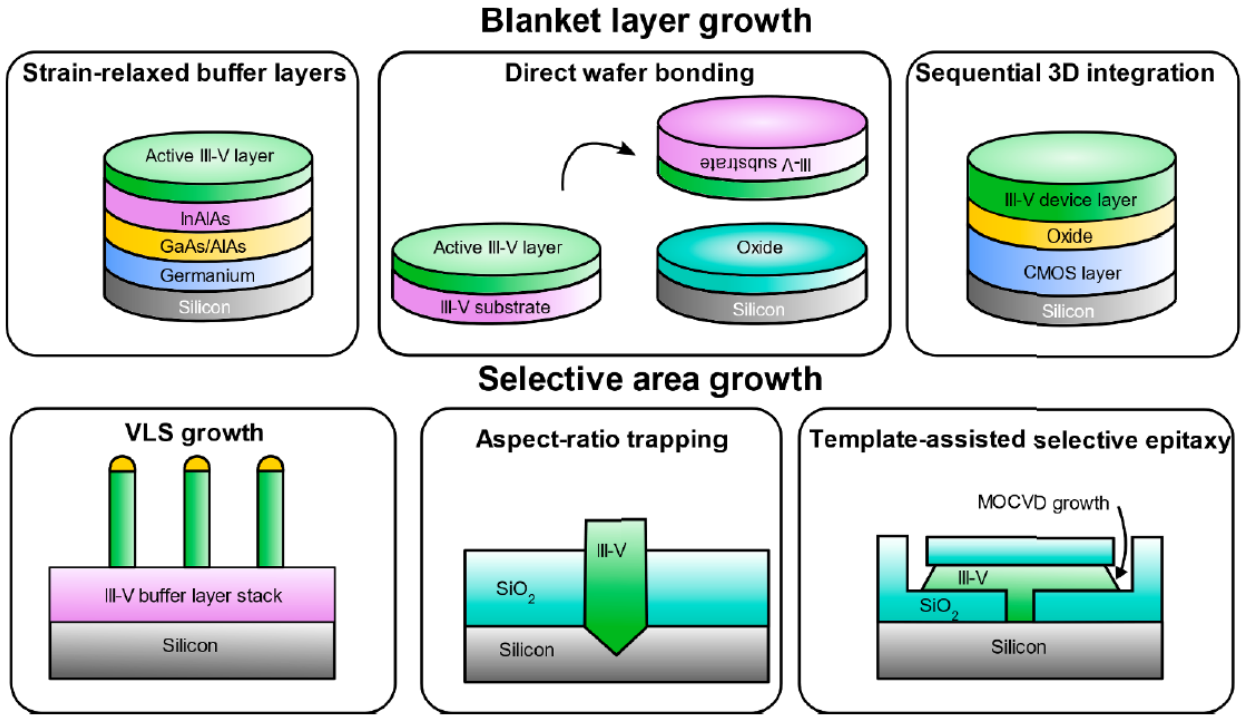


Fig. 1. Various approaches that have been explored to integrate III-V materials on Si substrates.

- **Patterned selective-area-growth (SAG) methods** provide a direct and potentially more flexible means to directly integrate disparate materials **if defectivity can be managed.**

- **Selective area epitaxy** is a local growth through a patterned amorphous dielectric mask (typically SiO_2 or Si_3N_4) deposited on a semiconductor substrate. Semiconductor growth conditions are selected to ensure epitaxial growth on the exposed substrate, but not on the dielectric mask.

Heterogeneous Material Integration on Si Platforms

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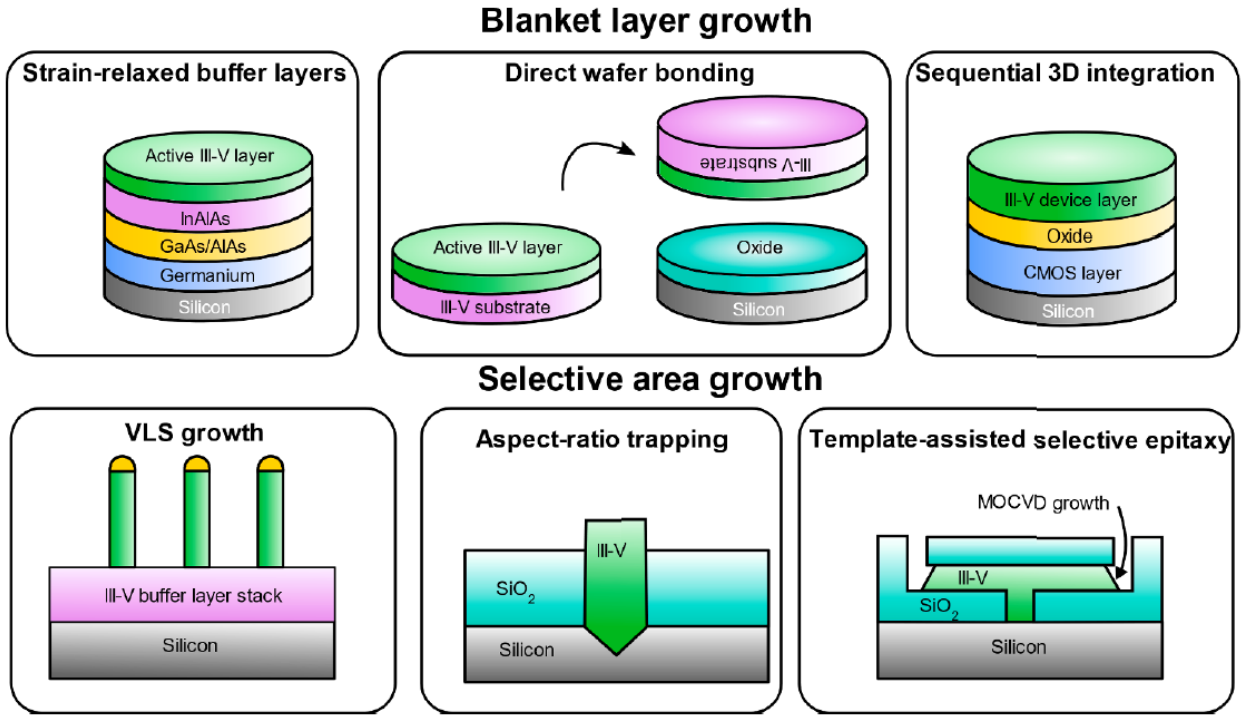
  - wafer bonding,

  - selective area growth,

  - aspect ratio trapping,

  - cyclic annealing.



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Selective Area Growth

- **Selective area growth (SAG) --> local growth of an epitaxial layer on a substrate through a patterned dielectric mask** (typically silicon oxide (SiO_2) or silicon nitride (Si_3N_4)**).**

⊂ **10 – 500 nm thick, covering a part of the substrate surface & leaving a defined Si surface – the "active area" – exposed for the growth of the active layers.**

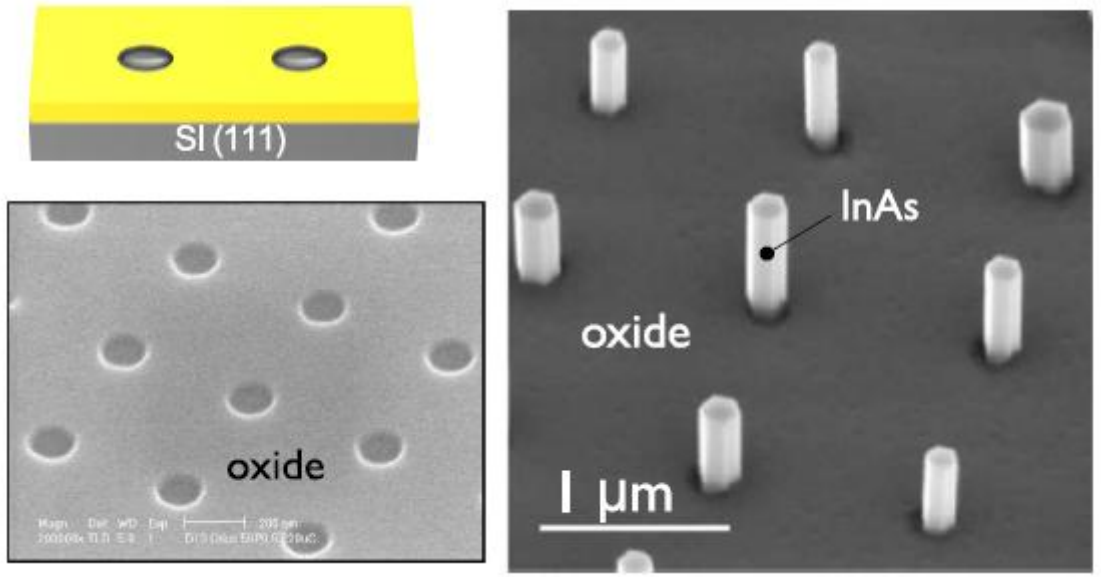
- Objective: to promote the growth of the layer only in the active area w/o nucleation on the mask

→ exclusively in a lithography defined area, this process enables alignment for the later device fabrication. But the **growth condition windows are reduced** to favour the growth rate locally

→ depending on the mask dimensions & the dielectric layer nature.

- **Crystalline quality, process selectivity, thickness, doping control, faceting need to be investigated.**

[N. Collaert et al., Microelec.Eng.132 (2015) 218]



Aspect Ratio Trapping

- **ART has been developed to integrate Ge or III-V devices with CMOS:** the buffer layer is thin (< 1 μm) to allow a standard CMOS back-end process, the technique has a low thermal budget, and the process can be applied to large wafers to allow integration into a CMOS process.

- **Ge or III-V material is epitaxially grown in high aspect ratio holes or trenches formed in dielectric layers on silicon.**

→ **In ART, dislocations are guided to the dielectric sidewalls and trapped, producing a low-dislocation density region at the top of the trench.**

- **Typically, the trenches are formed in thermally-grown SiO_2 by lithography & RIE etching** (in the fig., they are 800 nm deep, 200 nm wide and millimeters long).

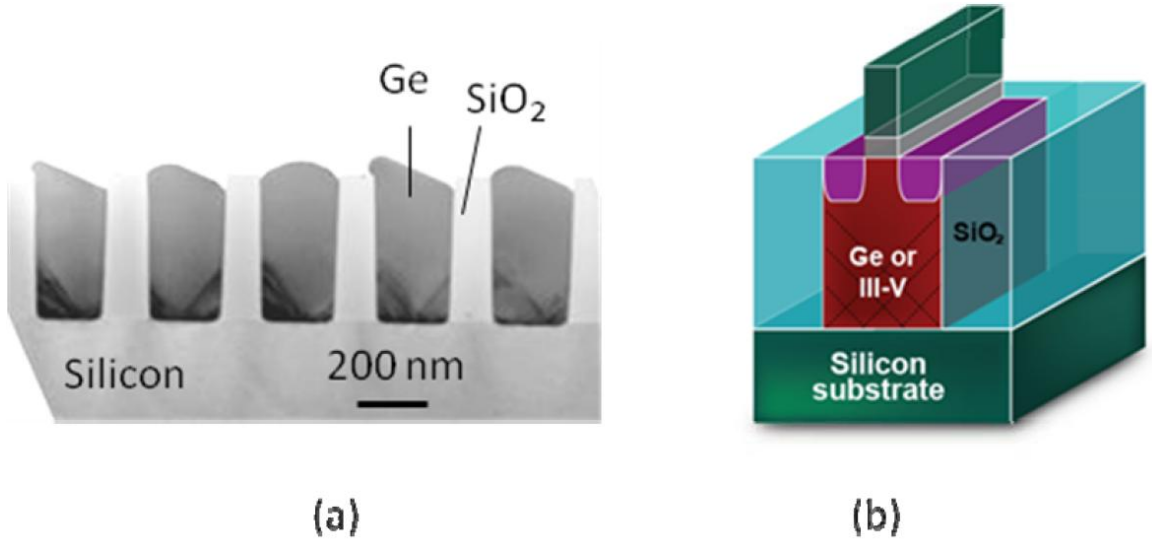
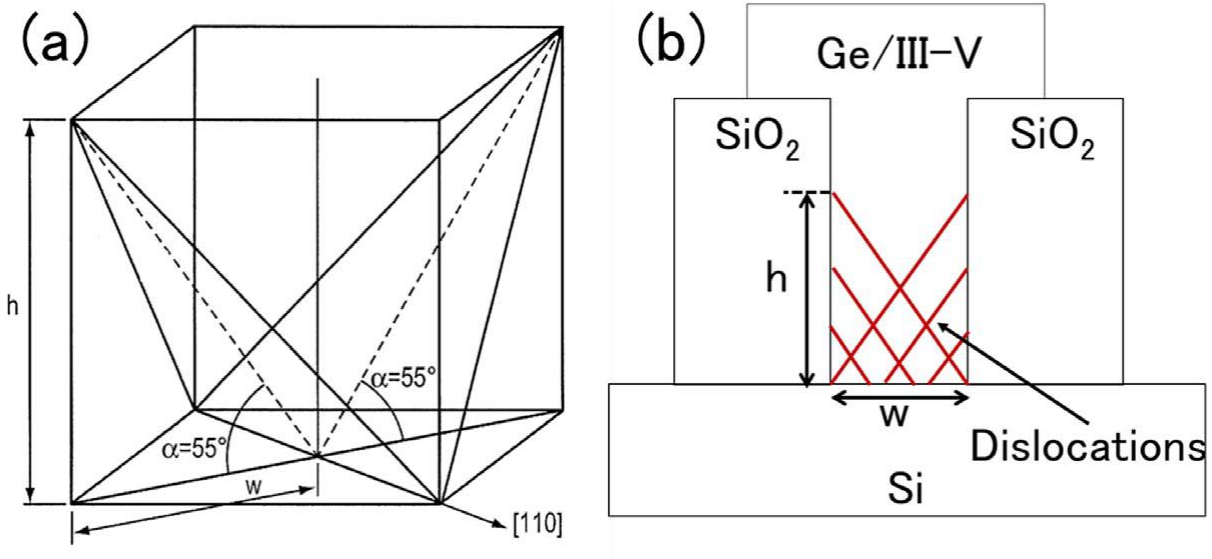


Figure 1. Depiction of Aspect Ratio Trapping using Ge in SiO_2 trenches. (a) XTEM of Ge epitaxially grown in SiO_2 trenches. Dislocations are formed at the Ge/Si interface because of the 4.2 % lattice mismatch between the Ge and silicon, but are trapped at the SiO_2 sidewall, yielding a region at the top of the trench with low dislocation density. (b) A depiction of a Ge or III-V MOSFET using ART.

[J. G. Fiorenza et al., ECS Transactions, 33 (6) 963-976 (2010)]

Aspect Ratio Trapping

- **The threading dislocations originating from the III-V/Si hetero-interface are guided to the oxide sidewalls, resulting in dislocation-free regions above a critical thickness.**
- The "trapping" of threading segments in the ART technique is attributed to the crystallographic geometry: in the {111}/<110> cubic slip system, misfit dislocations lie along the ⟨110⟩ directions in the (100) growth plane, while the threading segments rise up on the {111} planes in the ⟨110⟩ directions.



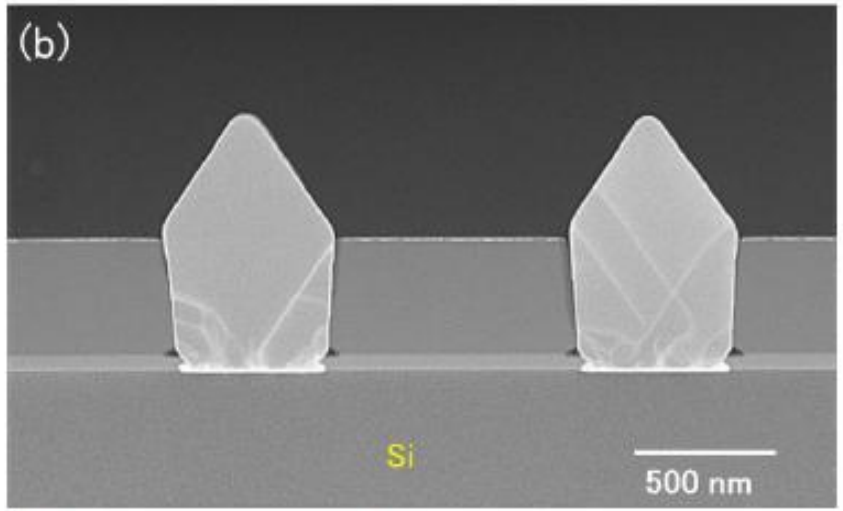


Fig. 10. (a) Tilted-view SEM image of GaAs selectively grown on a stripe patterned (001) Si substrate. (b) Cross-sectional annular dark field STEM image of GaAs-on-sub-micron-patterned-Si, showing the propagation of dislocations and stacking faults.

[Qiang Li et al., Progress in Crystal Growth & Characterization of Materials 63 (2017) 105–120]

Aspec

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- **Ge or III-V**
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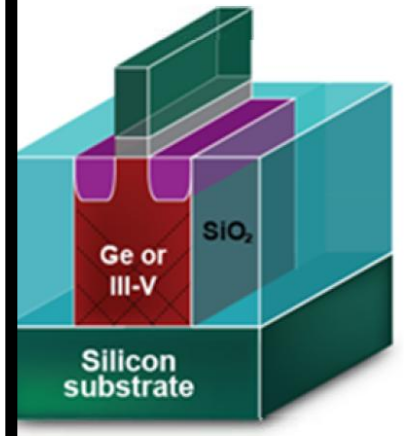


(b)

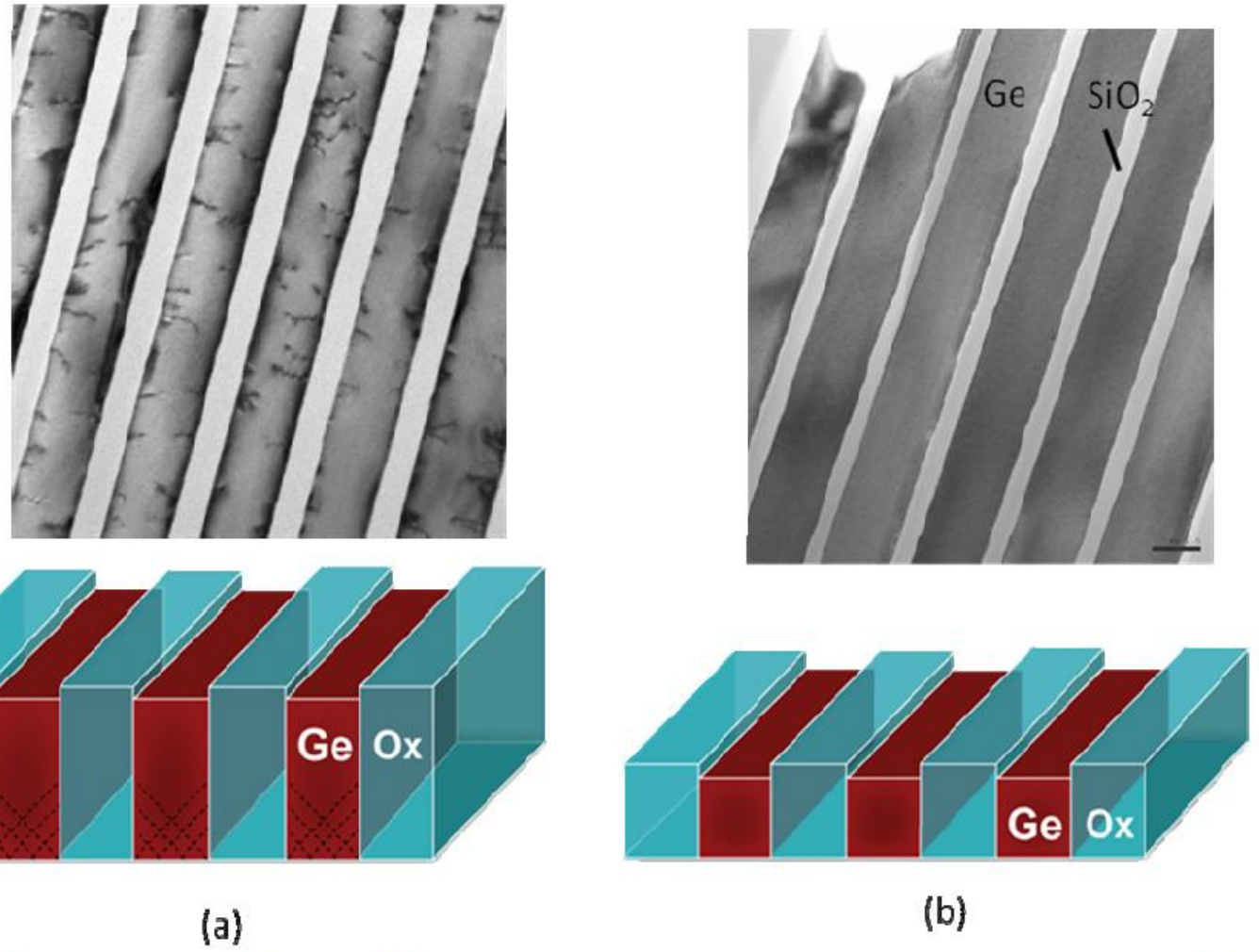


Figure 2. Depiction of Aspect Ratio Trapping using Germanium in SiO_2 trenches. (a) PVTEM of Ge in trenches in a sample thinned to the bottom of the trench. (b) PVTEM of Ge in trenches in a sample thinned to near the top of the trench.

in SiO_2 trenches. (a) XTEM of
e formed at the Ge/Si interface
d silicon, but are trapped at the
ith low dislocation density. (b)

(6) 963-976 (2010)]

The TEM images demonstrate that the threading dislocations are eliminated in the top of the trench for a large total area of material (~5 μm²)

Aspect Ratio Trapping

- ART is effective in reducing the surface TDD

→ **The surface dislocation density is reduced by 3 orders of magnitude from blanket Ge on Si.**

- The TDD decreases proportionately with the aspect ratio (trench height/trench width)

↪ the aspect ratio itself plays an important role in the mechanism by which ART reduces the TDD

- **ART is applicable to a variety of III-V materials (GaAs, InP).**

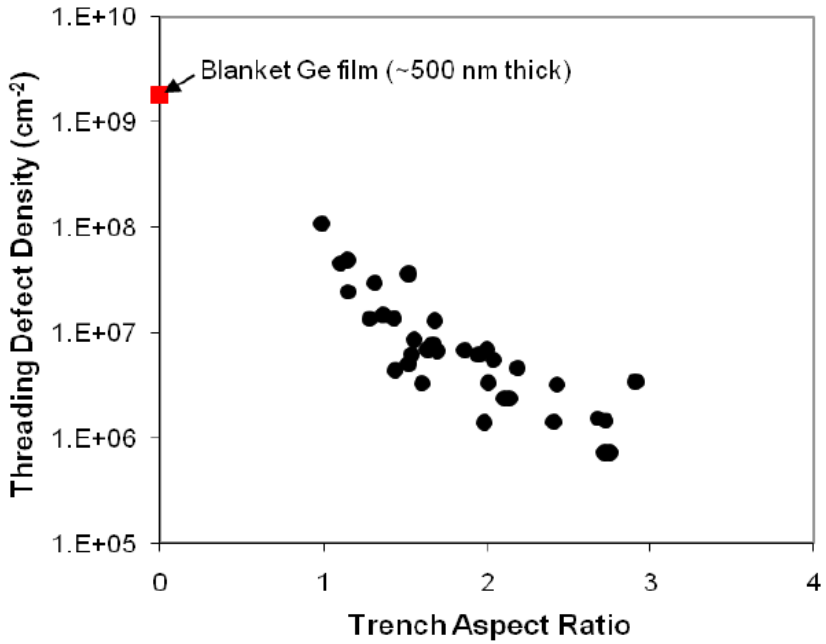


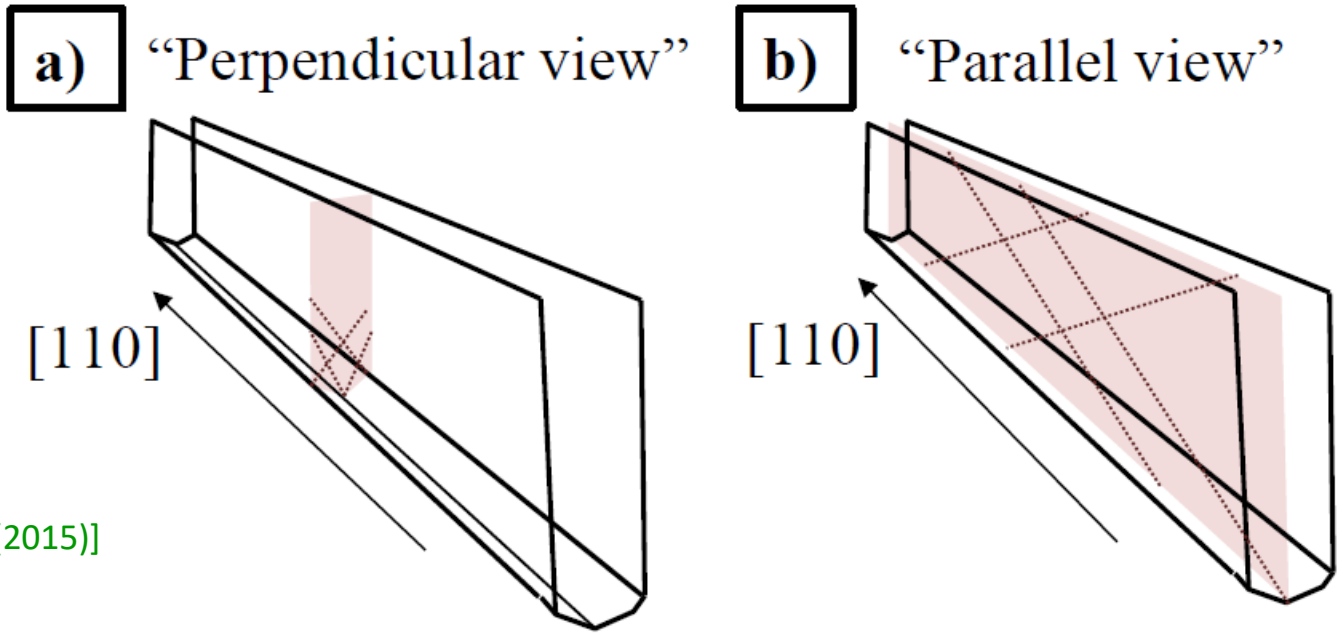
Figure 3. Threading dislocation density at the surface of a trench as a function of the trench aspect ratio.

[J. G. Fiorenza et al., ECS Transactions, 33 (6) 963-976 (2010)]

Aspect Ratio Trapping

- **Important reduction of the dislocation density within a thin deposited layer thickness** (few hundreds of nm)

- **The key challenge of this technique resides in the impossibility to trap the (111)-oriented defects along the parallel direction of the trench.**



[C. Merckling et al., ECS Transactions 66, 107 (2015)]

Figure 1. III-V selective area growth on Si(001) in trenches. (a) ***"Perpendicular view"*** *presenting an efficient trapping effect of (111)-oriented defects from the III-V/Si interface. (b)* ***"Parallel view"*** *where (111)-oriented defects are not trapped in the direction along the trench.*

Challenges in III-V/Si Hetero-Epitaxy

- **A specific defect is antiphase-domains (APD) due to the lack of inversion symmetry of III-V materials --> the sub-lattices are occupied by different atom species. The bonds are polar due to the difference in the ionicity of the constituent atoms.**

➡ **APDs are inherent to polar-on-non-polar growth. Single layer steps produce 2 domains in the III-V overlayer whereas double-layer steps do not.**

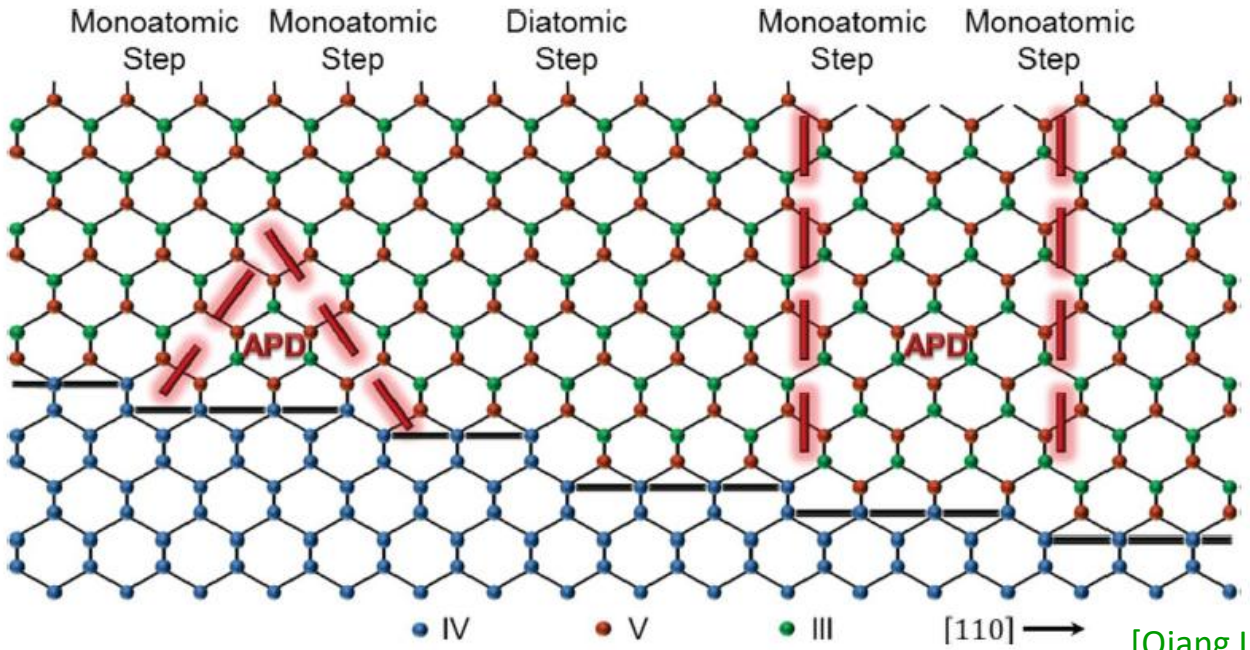
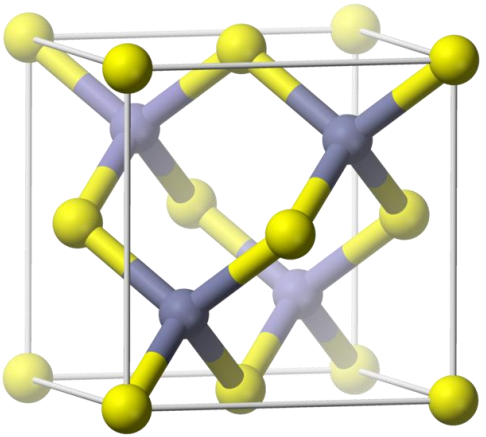
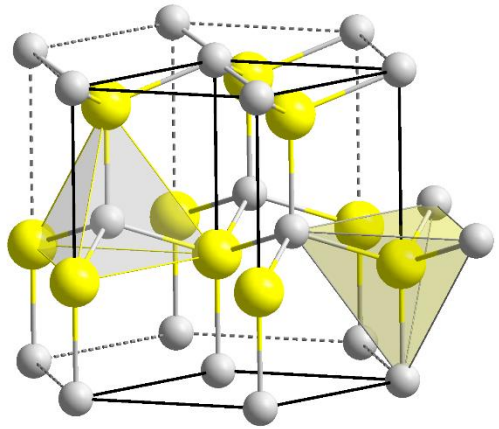


Fig. 2. Schematic down [1$\bar{1}$0], showing non-polar/polar interface between the group IV substrate and III-V epilayer. Monoatomic steps on the group IV substrate surface result in APBs, which are planes of V-V or III–III bonds. The APD can either self-annihilate (left) or rise to the surface (right). Diatomic steps on the substrate surface (center) do not result in APD formation. [27].





[Qiang Li et al., Progress in Crystal Growth & Characterization of Materials 63 (2017) 105–120]

Challenges in III-V/Si Hetero-Epitaxy

- **Development of surface preparation processes**
  - **Importance of the III-V/Si surface engineering to control the APD generation**
  - **Promotion of double-layer steps at the surface**
- Si (001) substrate (with a 0.15° misorientation in the [110] direction) is deoxidized in using NF_3/NH_3 remote plasma and then annealed (1 min–10 min) in an MOCVD reactor at high temperature (800 °C–950 °C) in H_2 ambient.

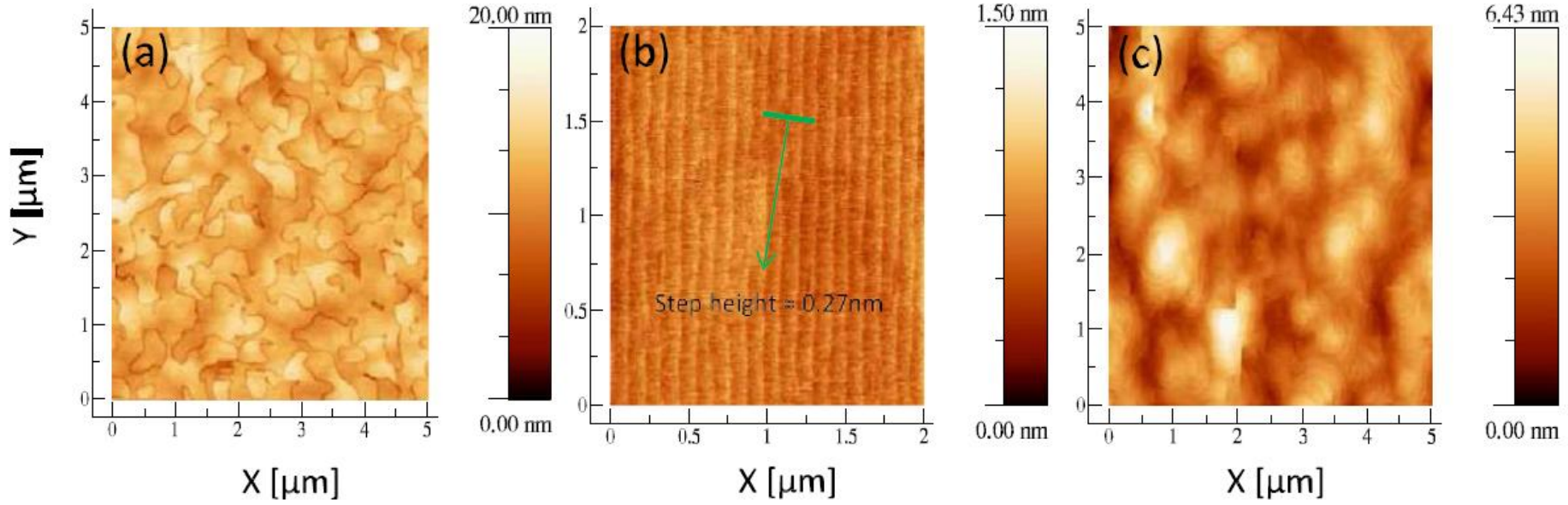


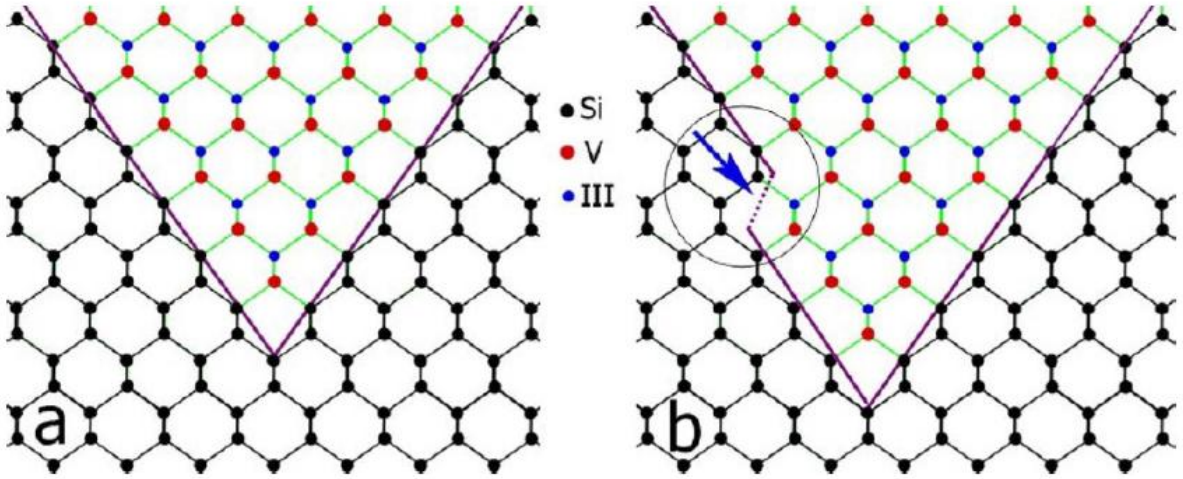
Fig. 5. (a) 5 × 5 µm² AFM image of 400 nm thick GaAs growth on un-optimized Si(001): High density of randomly oriented APBs; RMS roughness = 1.6 nm. (b) 2 × 2 µm² AFM image of 0.15° Si (001) after optimized preparation (800 °C–950 °C annealing under H_2). The surface is therefore mainly double-stepped. (c) 5 × 5 µm² AFM image of APBs-free 150 nm thick GaAs growth on optimized 0.15° Si(001): RMS roughness = 0.8 nm. [29].

[R. Alcotte et al., APL Mater. 4 (4) (2016) 046101]

Aspect Ratio Trapping Patterned Si

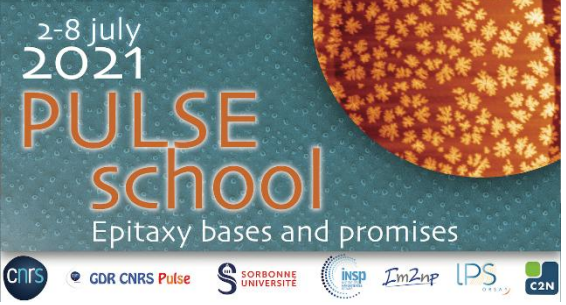
- **The use of {111} Si V-grooves in the ART growth process has been developped.**
- **The crystallographic alignment between the Si and III-V materials in the V-grooves avoids the introduction of APDs.**

  ⟹ **Crystallography analysis indicates that III-V SC on the two {111} facets of the "V-shape" have the same polarity.** In principle, the Si (111) surface can also have surface steps, as in the case of Si (001) --> **A single step on the Si (111) surface has the height of one Si (001) double-layer (0.31 nm). Such steps will not lead to the formation of APBs.**
- **III-V nucleation on Si (111) generates less defects as compared to nucleation on Si (001) & avoid the formation of the (111)-oriented defects along the parallel direction of the trench.**



A III-V lattice in the V-shape of Si with {111} facets along the [110] direction.

[Qiang Li et al., Progress in Crystal Growth & Characterization of Materials 63 (2017) 105–120]



SiGe & III-V technology

Beyond the Si Channel

- **Replacement of the Si channel in MOSFET with higher mobility (or injection velocity) materials.**
  - **Research efforts have focused on improving the effective mass (m*)**
    - **- strained Si MOSFET technology**

- **Beyond the traditional silicon channel materials:**
  - **- Ge-based materials for improving PMOS (low hole mass m*)**
  - **- III-V-based materials for improving NMOS (low electron mass m*)**
    - **$\mu \propto 1 / m^*$**

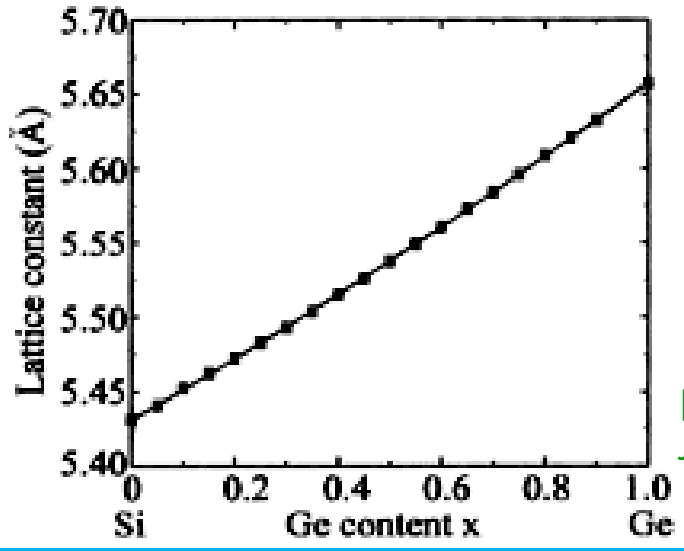
Strained Si MOSFET Technology

- **Strained Si channels have been introduced since the 90 nm node technology**
  → Use of epitaxial processes involving MOCVD or MBE growth

  ↪ higher speed operation (↗ μ) & improved current-voltage performances

- The carrier mobility increase, implemented by appropriate Si strain, provides **higher speed of the carriers** under the same conditions of polarization and a fixed oxide thickness.
  Or with the same current conditions in the channel, **thicker oxides and/or lower voltage supply can be used → relaxation of compromise between current, consumption & short channel effects**

- **Ge has a lattice constant of 5.658 Å with Si (5.431 Å) → up to 4.2% lattice-mismatch**



[Dismukes, J.P. et al., *JAP* **35** ,1964, 2899]

↪ **Use of an SiGe « template » to biaxially strain Si**
--> The tensile stress causes an increase in the lattice parameter of strained silicon

Strained Si MOSFET Technology

- **The strain leads to an energy splitting of the Si conduction band edge.**
- It lifts the six fold degeneracy in the conduction band and lowers the two perpendicular valleys (labeled Δ_2) with respect to the four in-plane valleys.
- **Electrons are expected to preferentially occupy the lower-energy valleys, reducing the effective in-plane transport mass.**
- **The energy splitting also suppresses intervalley phonon-carrier scattering, increasing the electron low-field mobility.**

RIM *et al.*: DEEP SUBMICRON STRAINED-Si N-MOSFET's

IEEE TRANS. ON ELECTRON DEVICES, 47, 1406, JULY 2000

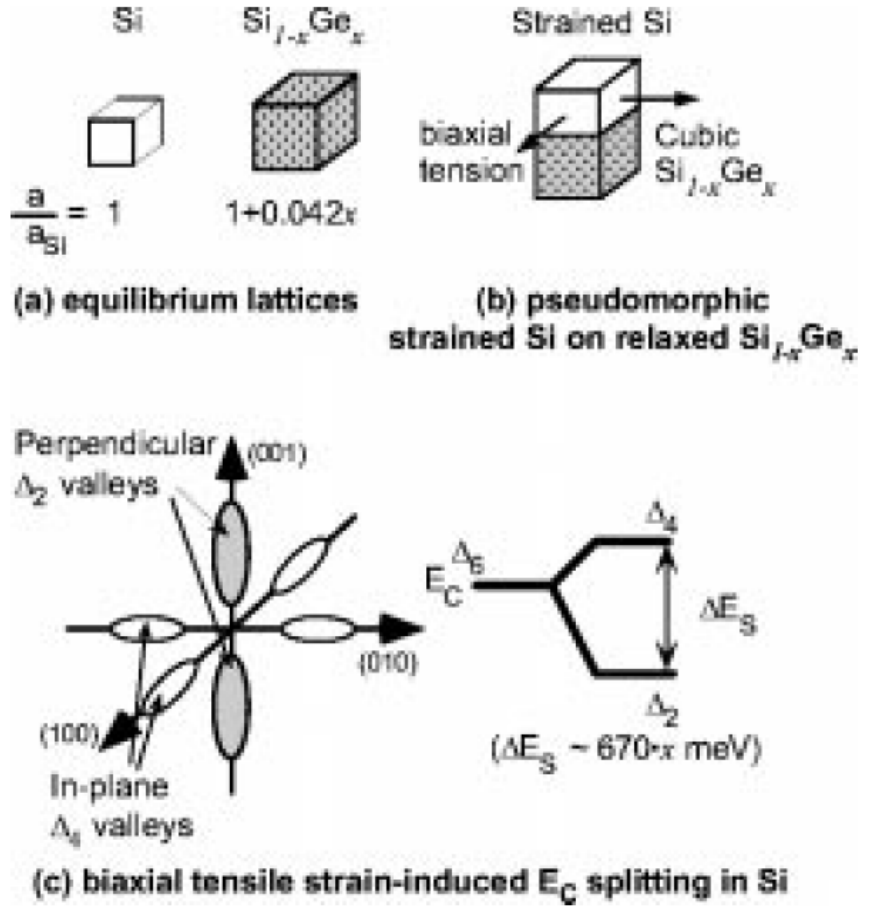


Fig. 1. Schematic illustrations of (a) equilibrium lattices, (b) peudomorphic strained Si on relaxed $Si_{1-x}Ge_x$, and (c) strain-induced conduction band splitting in Si.

Strained Si MOSFET Technology: Electron Transport

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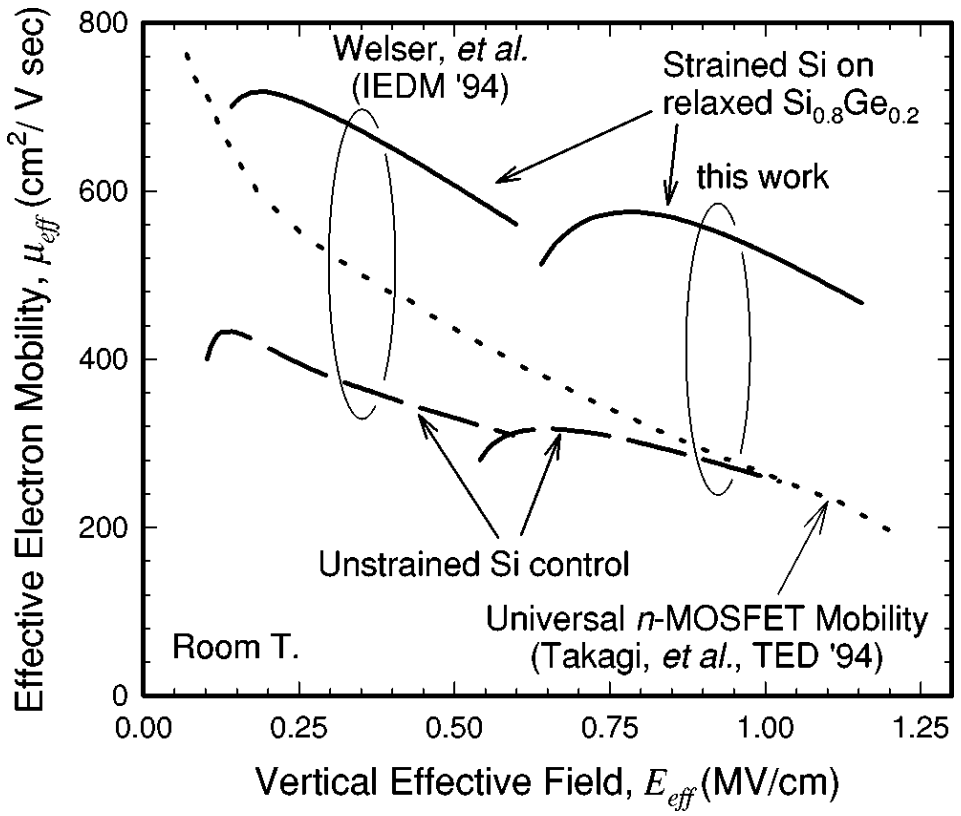
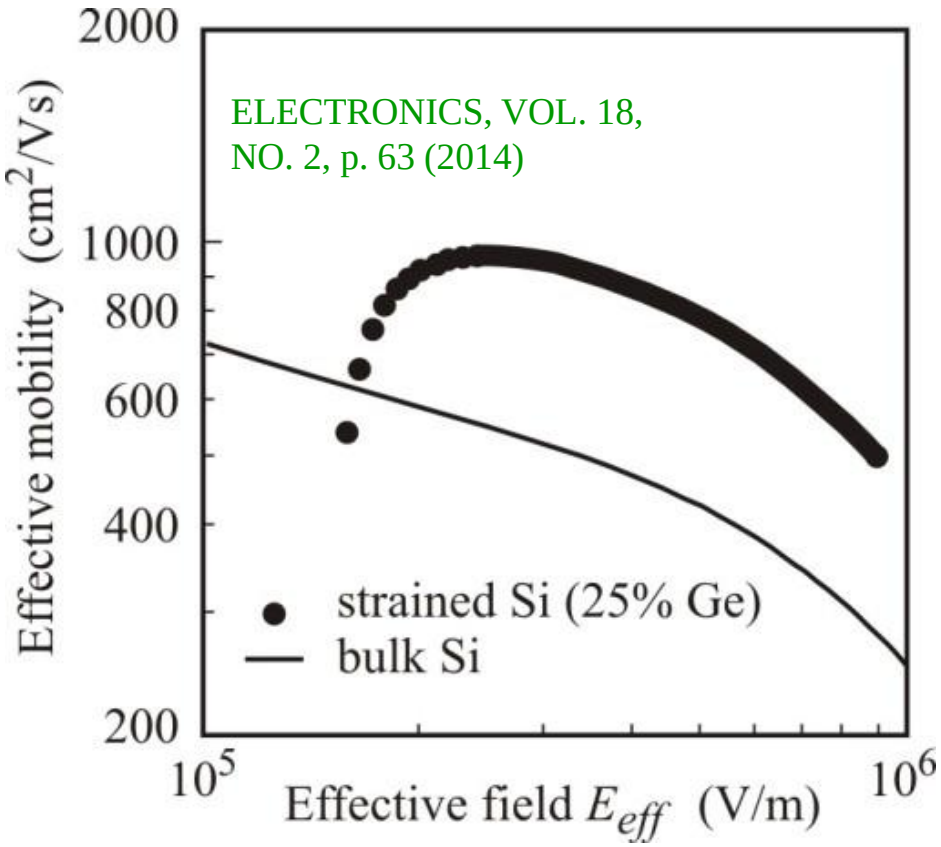


RIM *et al.*: DEEP SUBMICRON STRAINED-Si N-MOSFET's

JULY 2000



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SiGe channels

- Utilization of strained materials such as **strained Si for n-FET** and **strained SiGe for p-FET** are developped as a near-term technological solution.
- **SiGe layers pseudomorphically grown on Si substrates are under biaxial compressive strain.** SiGe layers on relaxed SiGe underlying buffers can have either biaxial compressive or tensile strain depending on the relative lattice mismatch between the two layers.

→ **Strain plays a role on the band structure and transport properties of SiGe channels**

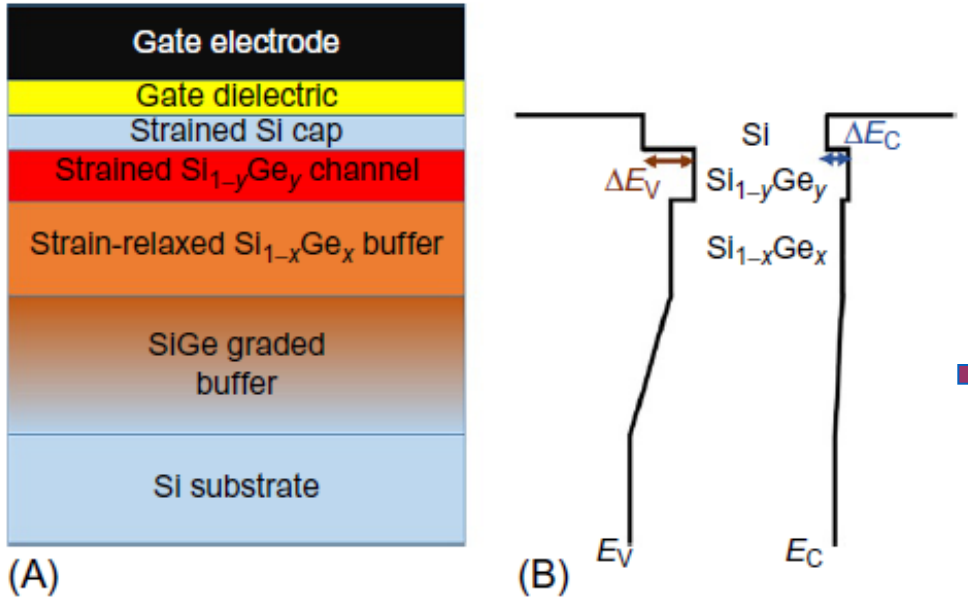


FIG. 6.1 (A) Structure and (B) band diagram of strained-Si/strained-$Si_{1-y}Ge_y$/relaxed-$Si_{1-x}Ge_x$ quantum-well heterostructure commonly used to characterize the transport in buried SiGe-channel pFETs.

- **For y > x, the buried $Si_{1-y}Ge_y$ layer is under biaxial compressive strain.**
- The strained-$Si_{1-y}Ge_y$ layer is capped with Si for surface passivation to control the interface traps for SiGe.

→ **The band alignment of strained Si and strained SiGe mostly confines the holes in the buried SiGe & the electrons in the strained-Si capping layer.**

Chapter 6 – SiGe Devices, Pouya Hashemi and Takashi Ando
High Mobility Materials for CMOS Applications.
https://doi.org/10.1016/B978-0-08-102061-6.00004-5

SiGe channels: Hole Transport

- **Hole mobility monotonically increases with increasing Ge content in the biaxially strained-SiGe.** Adjusting the Ge content in the channel and the buffer, a wide range of mobility values can be achieved ➡ **mobility enhancements up to 10x over (100)-Si.**
- **Moreover, extremely high hole effective mobility numbers > above 1000cm²/V.s have been measured for buried-channel strained-$Si_{1-y}Ge_y$ quantum wells.**

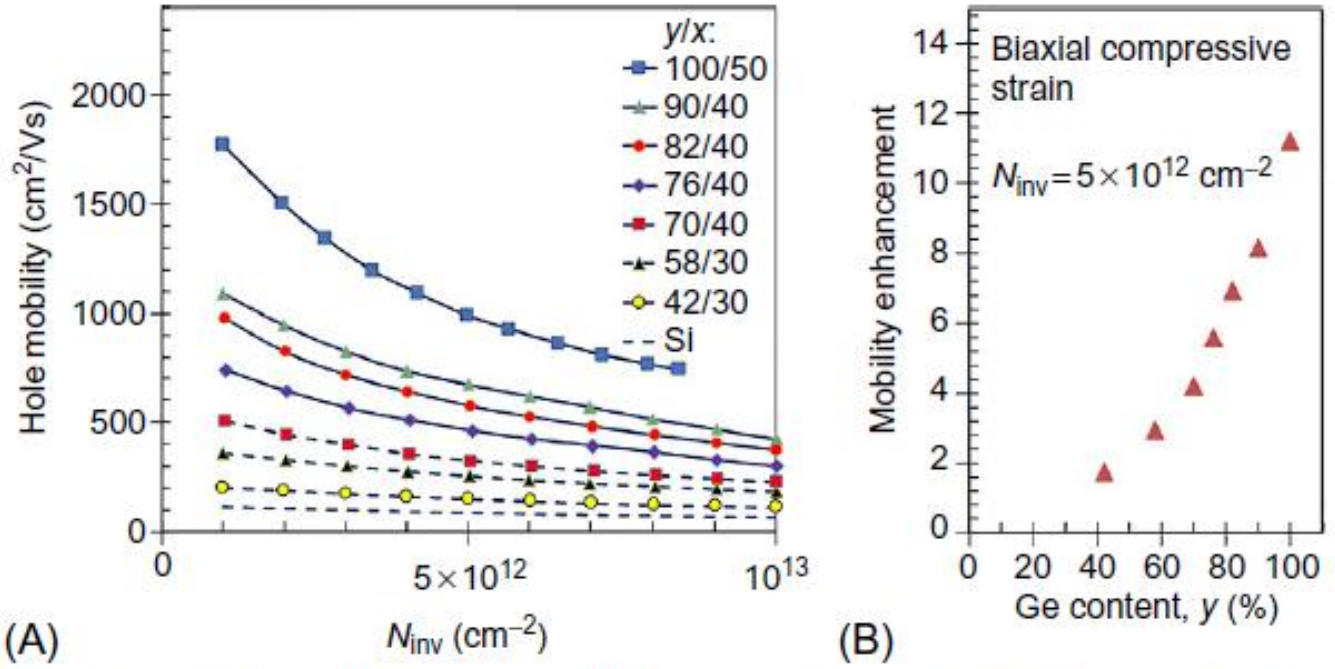


FIG. 6.2 (A) Measured effective hole mobility versus N_{inv} for strained-Si/strained-$Si_{1-y}Ge_y$/relaxed-$Si_{1-x}Ge_x$ quantum-well heterostructures for various y/x. (B) Hole mobility enhancement factor over Si versus channel Ge fraction. *(Data from J.L. Hoyt and C. Ni Chleirigh, Massachusetts Institute of Technology, with permission.)*

- The effective mass of SiGe is a strong function of Ge fraction, strain state (compression or tension), and strain type (uniaxial, biaxial).

SiGe channels: Hole Transport

- The biaxial strain is shown to lift the degeneracy of the heavy-hole and light-hole subbands in the valence band, in addition to the effective mass reduction.
- **On the other hand, the theory suggests that the uniaxial compressive strain can further reduce the hole effective mass and is the optimum strain for the hole transport.** The calculated hole effective mass of relaxed and uniaxially strained SiGe, lattice matched to Si, for various Ge fractions and surface orientations.

  → **The hole effective mass decreases with increasing Ge content and uniaxial strain.**

- **A way to achieve uniaxial strain is to start from globally biaxial strained substrates and pattern them to high-aspect-ratio fingers or bars leading to strain relaxation along one direction.**

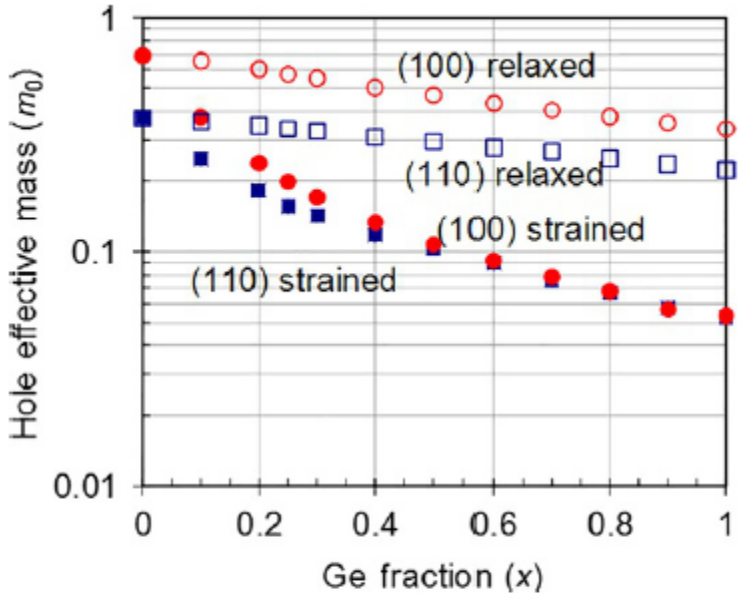


FIG. 6.3 Simulated hole effective mass as a function of Ge fraction for relaxed and uniaxial compressively strained $Si_{1-x}Ge_x$ (lattice matched to Si), with (100) and (110) surface orientations. *(Reproduced with permission from K. Ikeda, M. Ono, D. Kosemura, K. Usuda, M. Oda, Y. Kamimuta, et al., High-mobility and low-parasitic resistance characteristics in strained Ge nanowire pMOSFETs with metal source/drain structure formed by doping-free processes, in: 2012 Symposium on VLSI Technology (VLSI Technology) Digest of Technical Papers, 2012, pp. 165–166. Copyright 2012 IEEE.)*

Integration of devices on a Si CMOS platform

- **Demonstration of a GaAs MOSFET on silicon using ART.**

→ The transfer characteristics showed a peak mobility of 503 cm²/Vs, which was similar to the value seen on a GaAs MOSFET made on a bulk GaAs substrate using the same MOSFET fabrication process, and which exceeds the silicon universal mobility curve.

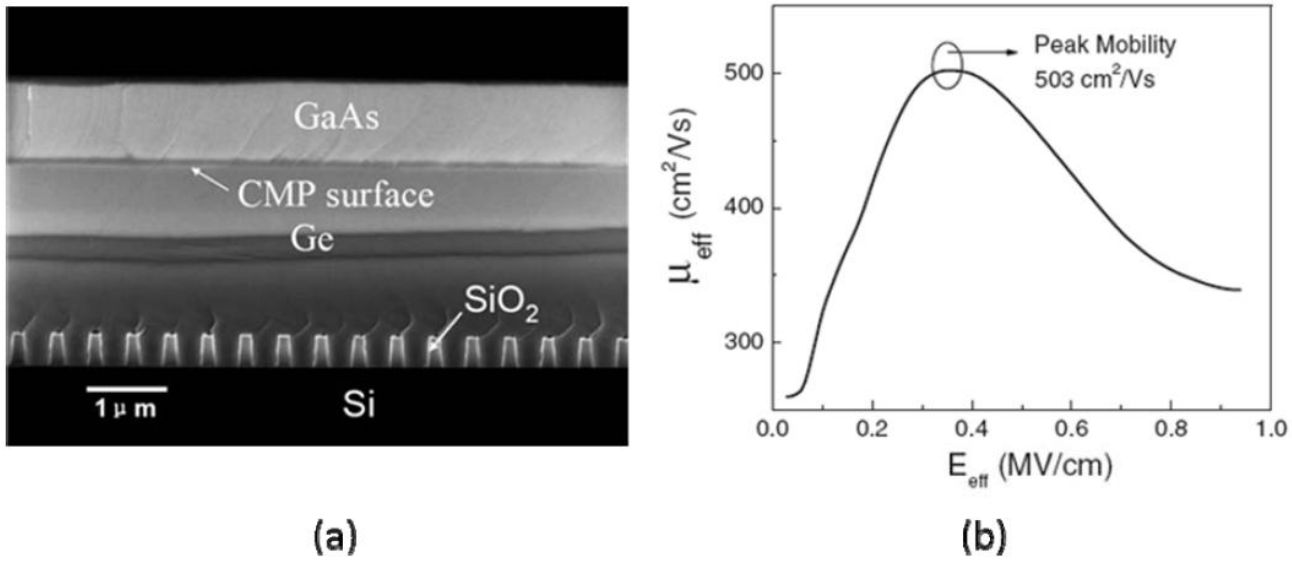
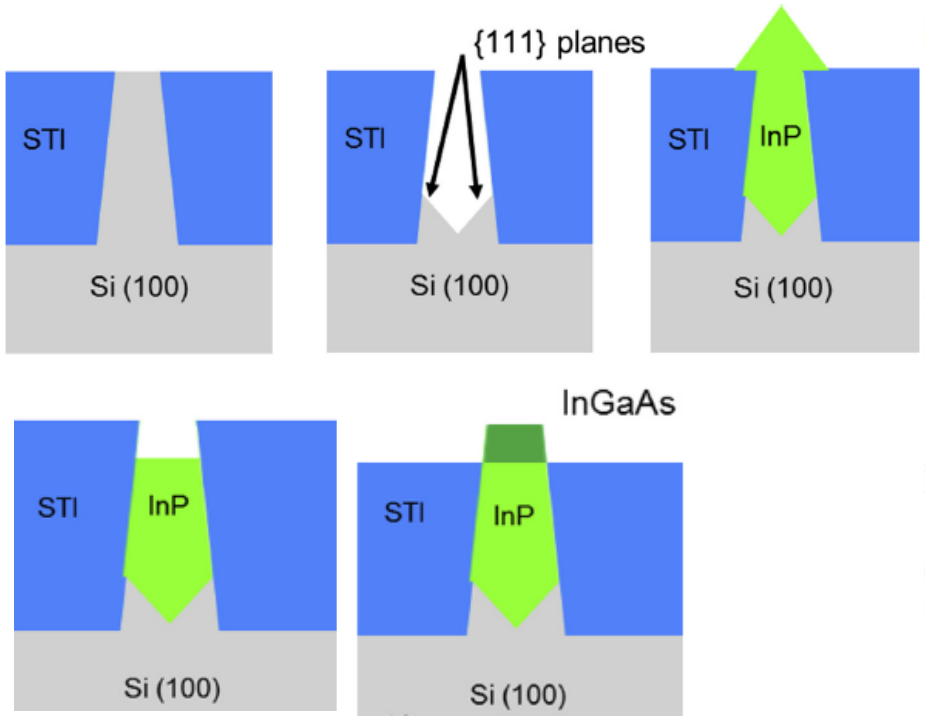


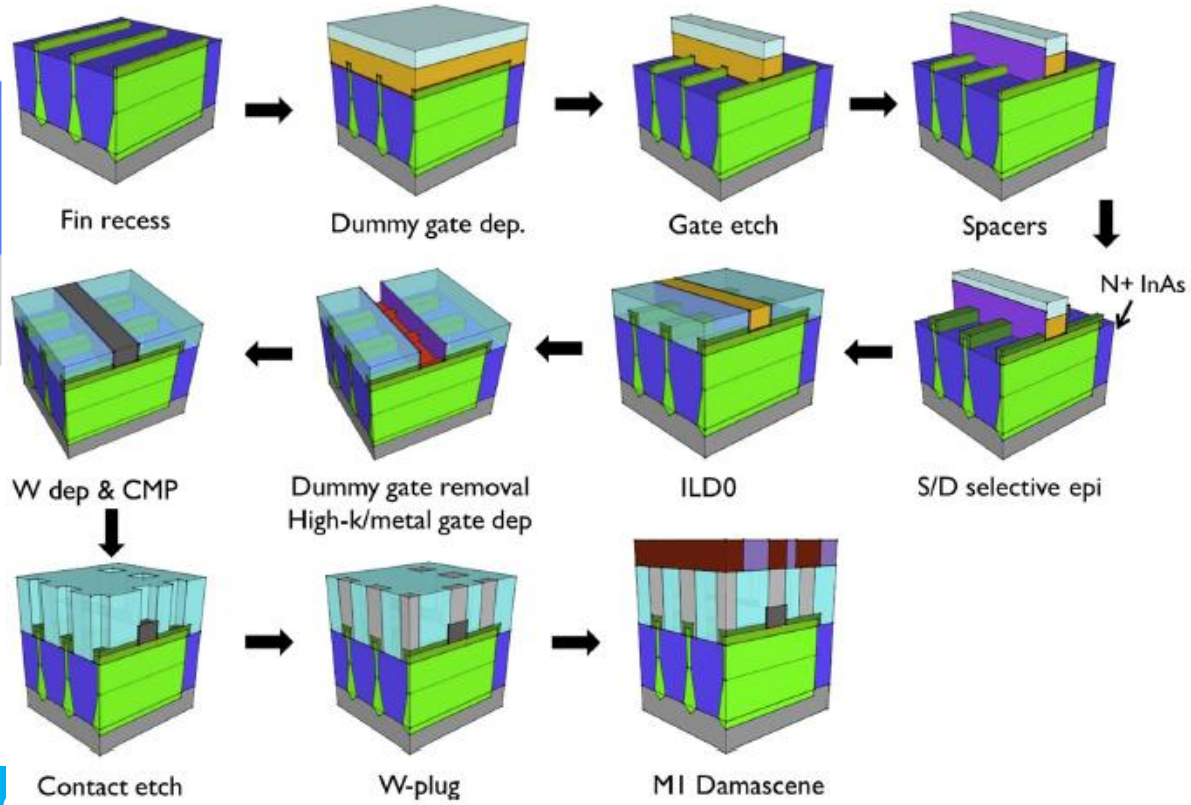
Figure 12. (a) XSEM of the epitaxial structure and (b) output characteristics of a GaAs MOSFET fabricated on silicon using ART.

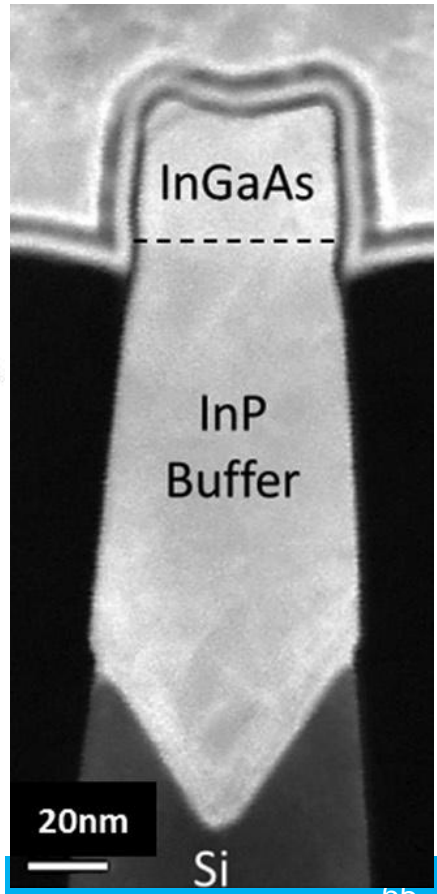
[Y. Q. Wu et al., Appl. Phys. Lett. 93, 242106 (2008)]

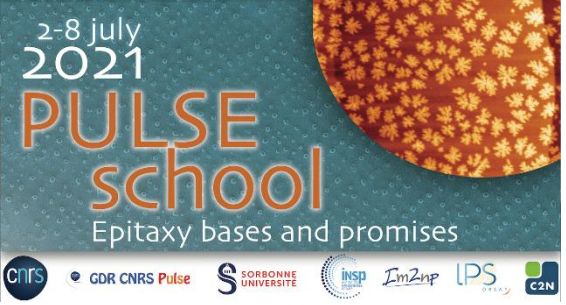
InGaAs-based channel FinFET

- **Initiation of the growth on the Si {111} planes and use of an InP buffer layer.**
- **Steps of chemical mechanical polishing (CMP) / chemical etching for InP recess.**
  Growth of the $In_{0.53}Ga_{0.47}As$ channel layer --> the depth of the InP recess determines the thickness/height of the InGaAs channel. [N. Waldron et al., Solid-State Electronics 115, 81 (2016)]
  The STI oxide is recessed and then follows a typical Si Fin.





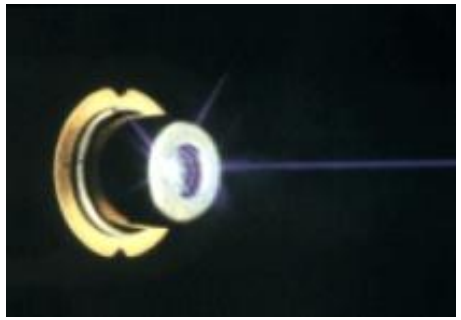




GaN Electronics

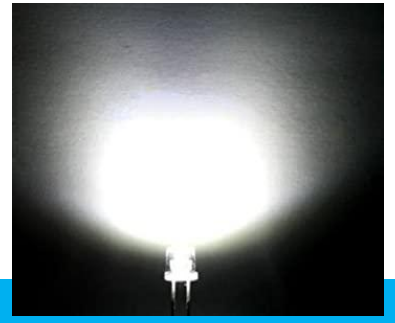
Why GaN ?

Optoelectronic Applications:

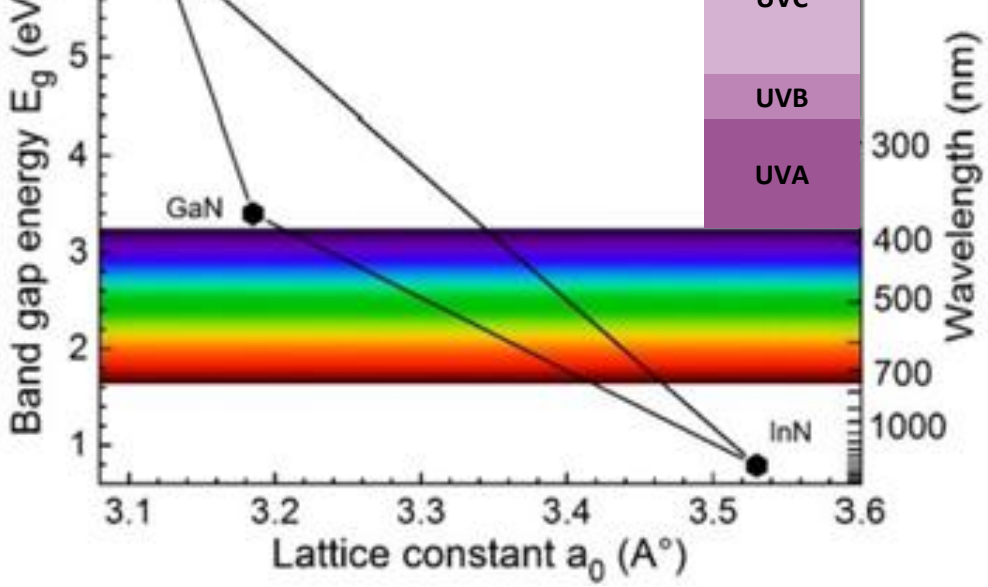


LED, lasers, …

- **Wide band Gap semiconductors (AlN, GaN)**
- **From IR to UV**
- **Wide range of applications**



→ **White light LED**



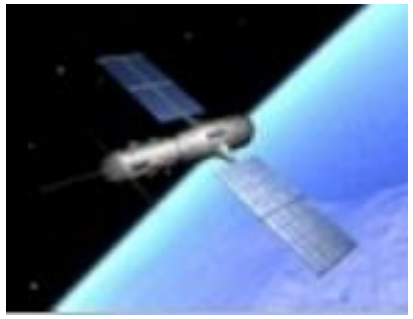
The Nobel Prize in Physics 2014

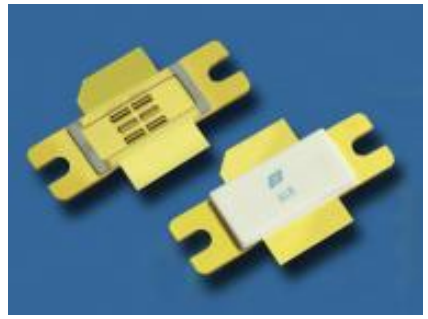
Isamu Akasaki, Hiroshi Amano, Shuji Nakamura

" For the invention of efficient blue LEDs which has enabled bright and energy-saving white light sources "

Why GaN ?

Electronic Components:





Telecommunication, radars, power electronics,…

Properties (300 K)	Si	InP	GaAs	4H-SiC	GaN
Band Gap Energy (eV)	1.12	1.35	1.43	**3.25**	**3.43**
Breakdown Field F_{cl} (MV/cm)	0.3	0.45	0.4	**3**	**3**
Electron Saturation Velocity v_s (x10^7 cm/s)	1.1	1	1	**2**	**1.8**
Thermal Conductivity Θ_K (W/cm.K)	1.5	0.7	0.5	**4.9**	**1.5**

$$\longrightarrow P_{\max} \propto I_{\max} \times V_{cl}$$

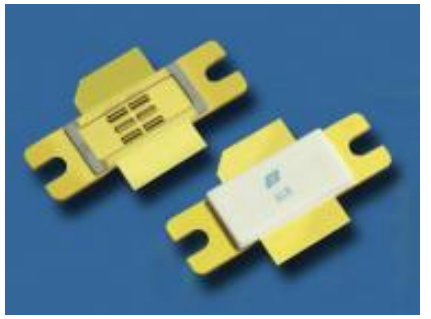
$$\longrightarrow f_c \propto v_{sat}$$

(Cut-off frequency)

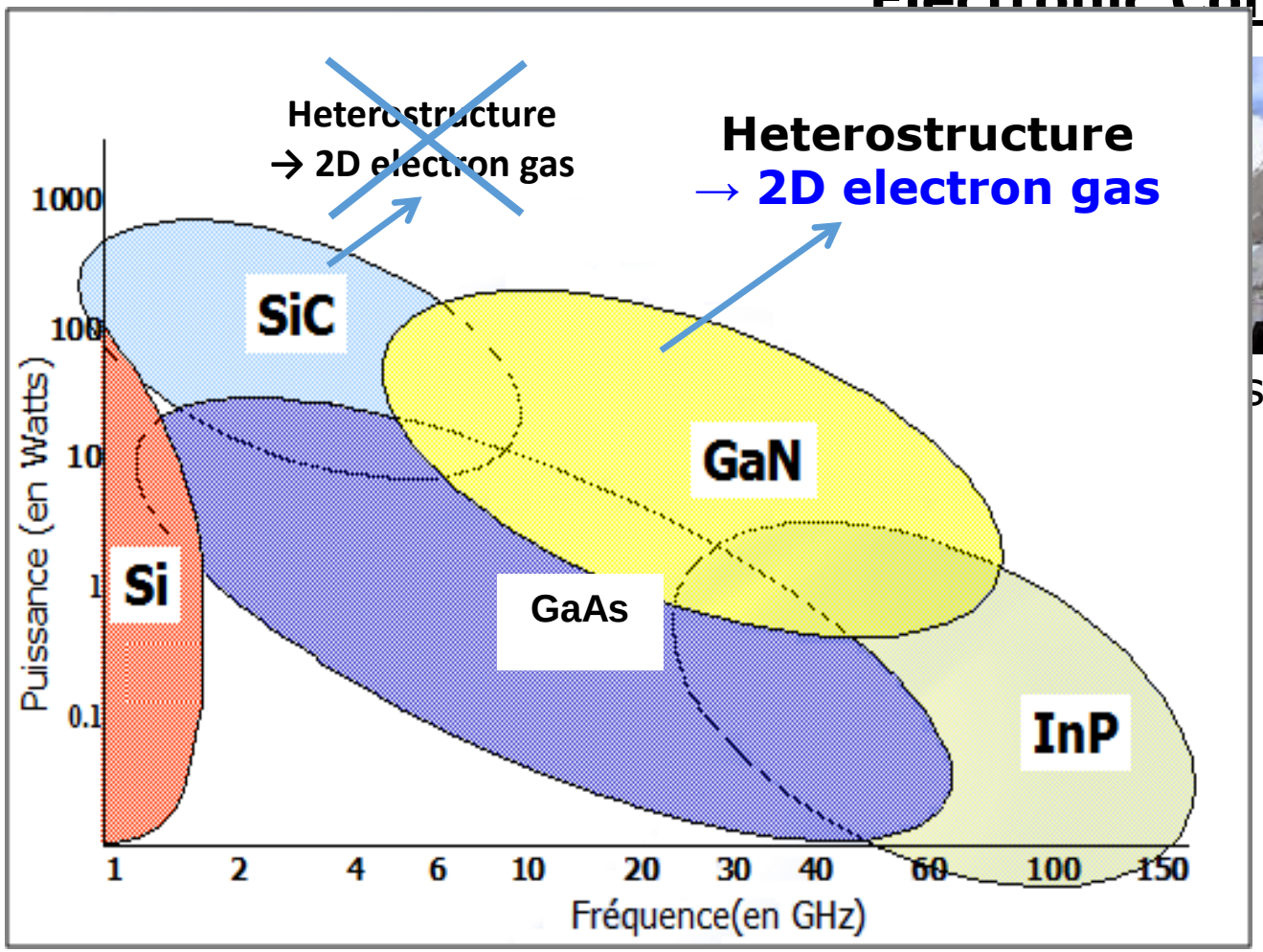
GaN --> high breakdown field, good thermal conductivity, high electron saturation velocity

Why GaN ?

Electronic Components:



s, power electronics,…

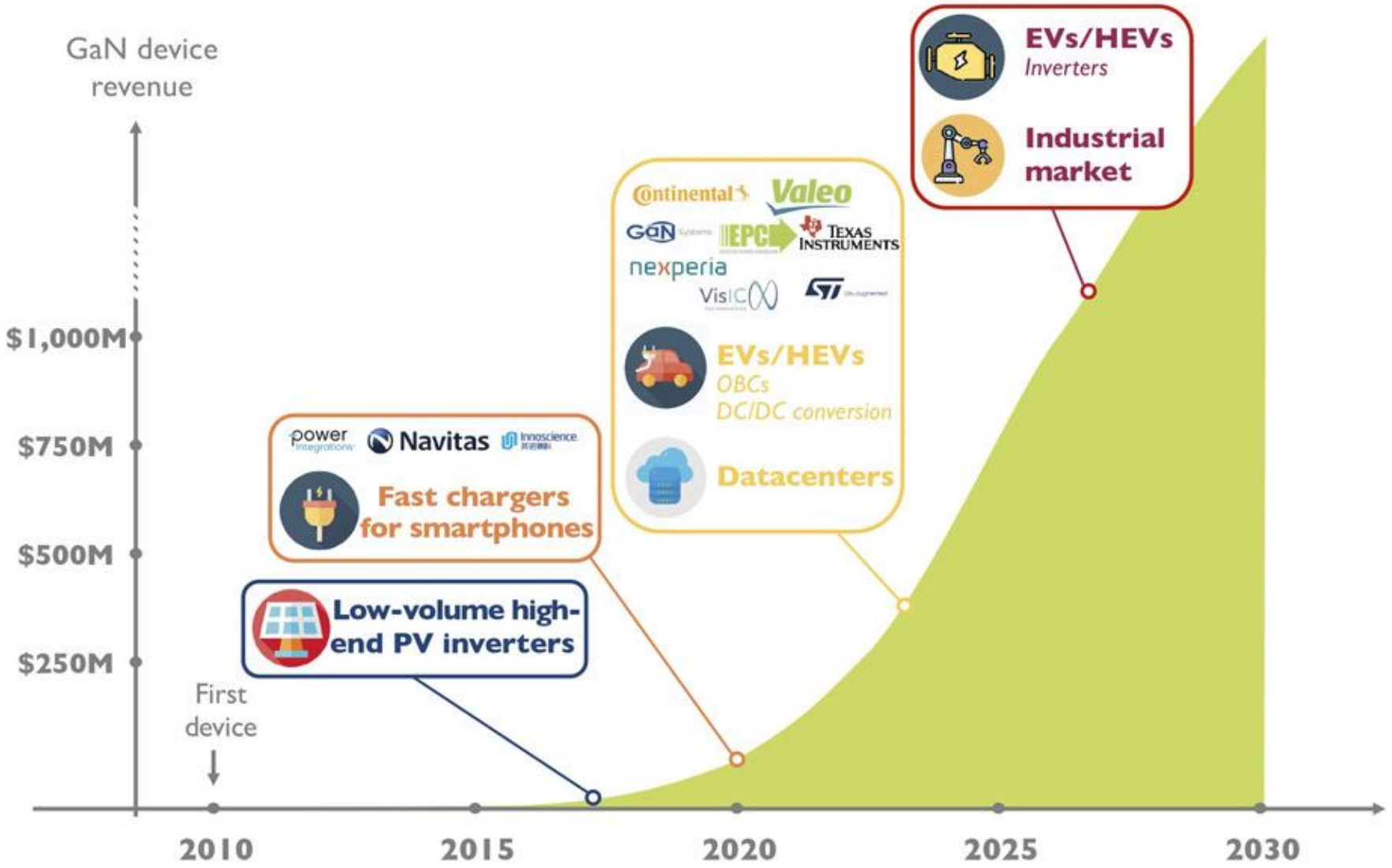


GaN: well-adapted materialfor high-frequency high-power electronic components

Roadmap for GaN power devices

(Source: GaN Power 2021: Epitaxy, Devices, Applications and Technology Trends report, Yole Développement, 2021)

➡ **New players have entered the market with GaN-on-Si** enhancement-mode (E-mode) **high-electron-mobility Transistor (HEMT) technology**



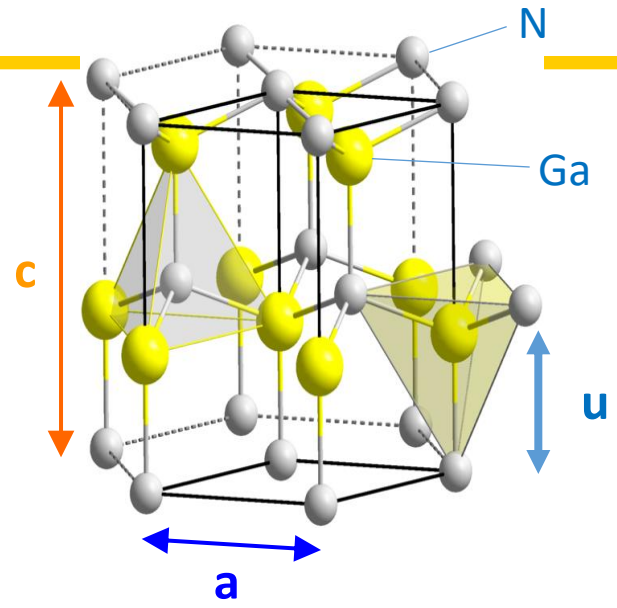
www.semiconductor-today.com/news_items/2021/may/yole-100521.shtml

GaN Crystal Structure & Polarization

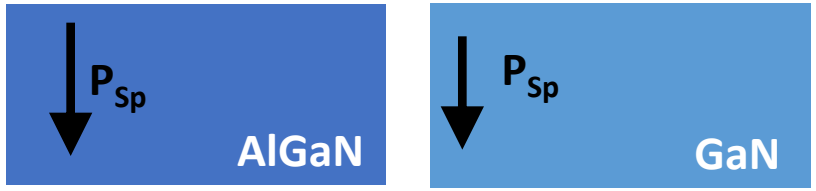
- **Wurtzite structure with two hexagonal sublattices**
- **A unique c-polar axis**
- **Non ideal wurtzite structure**

  → **the tetrahedron is distorted**

  c shorter = tetrahedron compressed along c



- **Spontaneous polarization (P_{sp})**
  - **The direction depends on the film polarity (Ga or N polar)**



(Ga, Al) polar

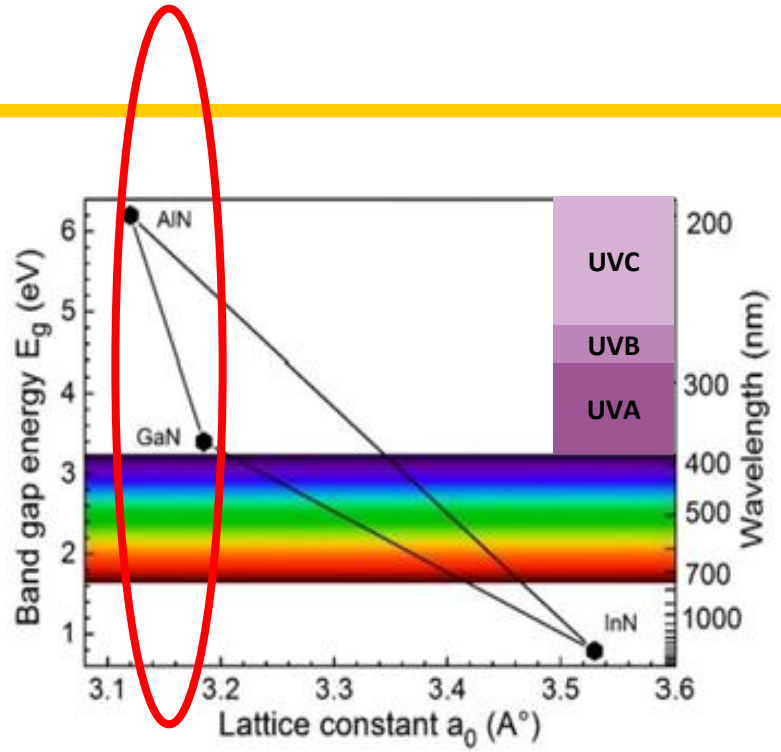
	a(nm)	c(nm)	c/a	u/c
GaN	0.3189	0.5185	1.626	0.377
AlN	0.3113	0.4982	1.600	0.382
InN	0.3538	0.5703	1.612	0.377

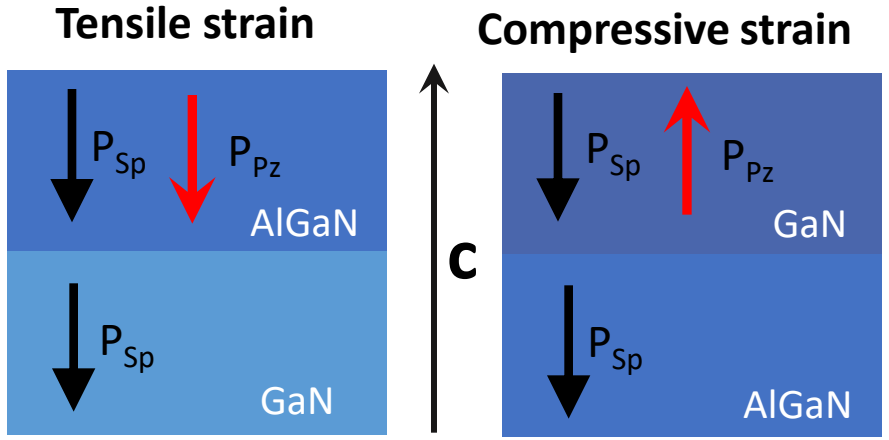
Ideal wurtzite

c/a	c/u
1.633	2.666

Polarization in Heterostructures

- **Wurtzite structure with two hexagonal sub-lattices**
- **A unique c-polar axis**
- **Piezoelectric polarization (P_{pz})**
  - **Due to the epitaxial strain (the direction depends on the type of strain)**
- **Total polarization ($P = P_{sp} + P_{pz}$)**





Polarization in a AlGaN/GaN Heterostructure

➢ **Total polarization ($P = P_{sp} + P_{pz}$)**

Heterostructure

↓

Different total polarization

↓

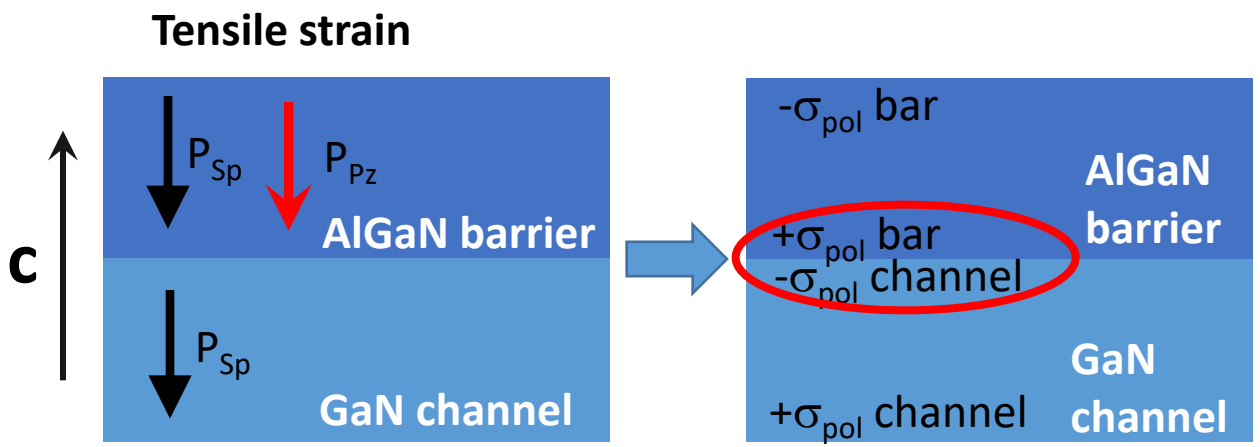
Charge densities at the interface

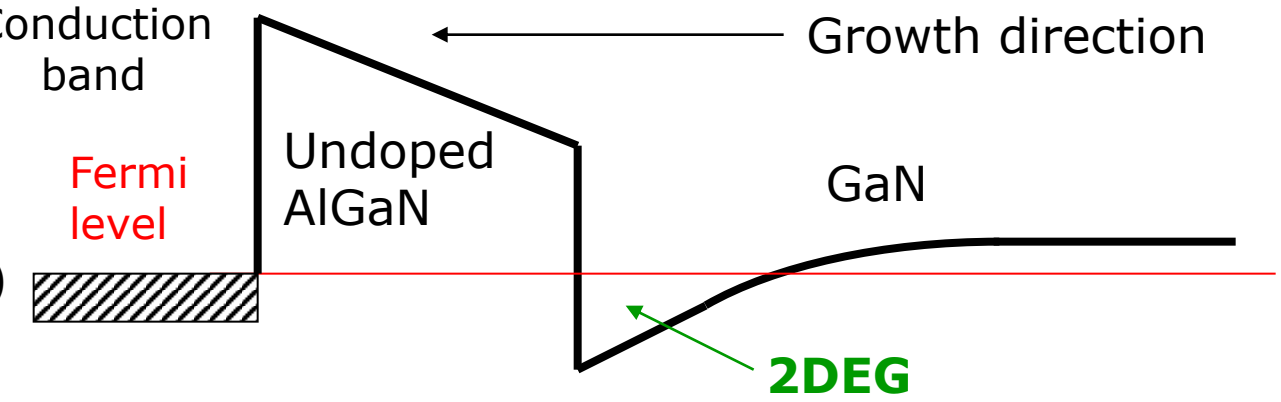
↓

Internal electric field

↓ $F = \Delta P = (P_{bar} - P_{cha})/\varepsilon\varepsilon_0 = \sigma/\varepsilon\varepsilon_0$

Band structure bending





HEMT heterostructure:
A cladding barrier (larger gap than GaN) is grown on the GaN channel

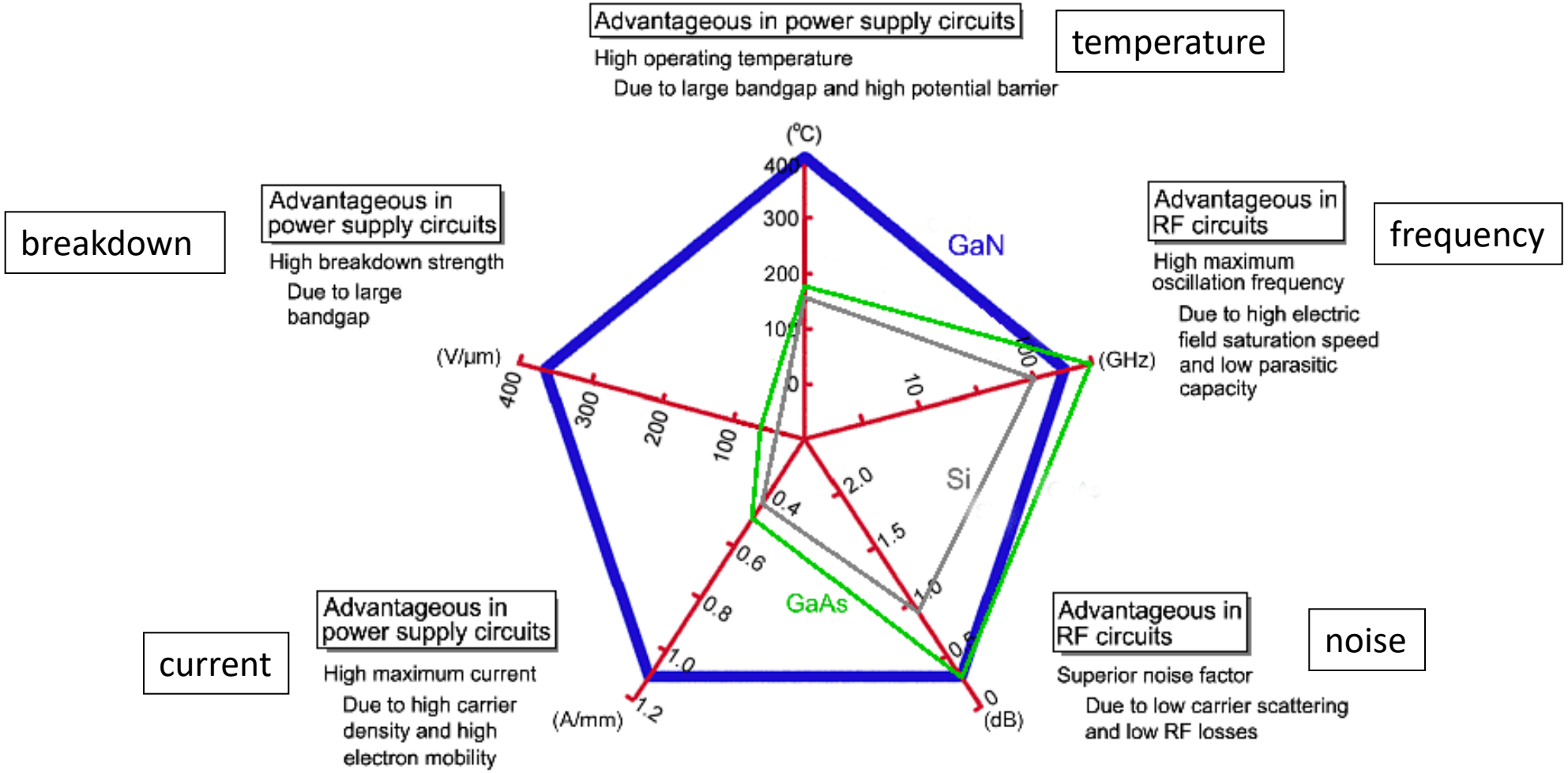
At the AlGaN/GaN interface: polarization difference and conduction band discontinuity

formation of a triangular QW → 2D electron gaz (2DEG)

Electron density $N = \sigma / q$

Comparison of Si, GaAs and GaN

- **Comparison of the main properties for power and microwave applications**



https://sudonull.com/post/29796-Why-silicon-and-why-CMOS

Hetero-Epitaxial Growth of GaN on Si

- **Lack of GaN native substrates:**
  - limited supply & very expensive (few thousand $)

→ **Growth on Si (less than 100 $ for 200 mm wafer)**
--> large lattice-mismatch & thermal mismatch

Table 1
Material properties of GaN, AlN, Si, SiC, and sapphire (the given thermal expansion coefficient is an averaged value and might differ significantly at very low and at high temperatures) [7–9, 13–18]

material	a (Å)	c (Å)	thermal conductivity (W/cm K)	thermal expansion coefficient in-plane (10^{-6} K^{-1})	lattice mismatch GaN/substrate (%)	thermal mismatch GaN/substrate (%)
GaN	3.189	5.185	1.3	5.59	–	–
AlN	3.11	4.98	2.85	4.2	2.4	25
Si(111)	5.430	–	1–1.5	2.59	–16.9	54
6H-SiC	3.080	15.12	3.0–3.8	4.2	3.5	25
sapphire	4.758	12.991	0.5	7.5	16	–34

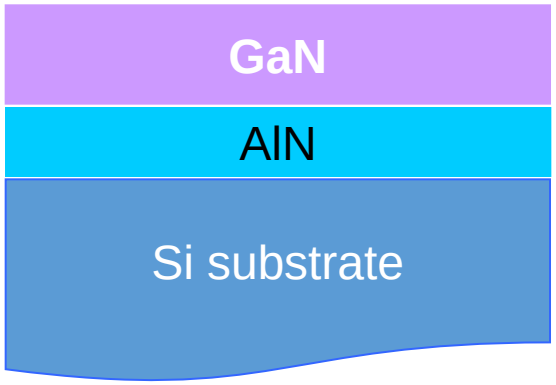
Hetero-Epitaxial Growth of GaN on Si

- **Main difficulties:**

- the "melt-back etching" --> reaction between Ga & Si at high temperature

If Ga comes into contact with Si during growth, this leads to melt-back etching which generates large defects in the GaN structures.

Use of a blocking layer between GaN and Si --> AlN



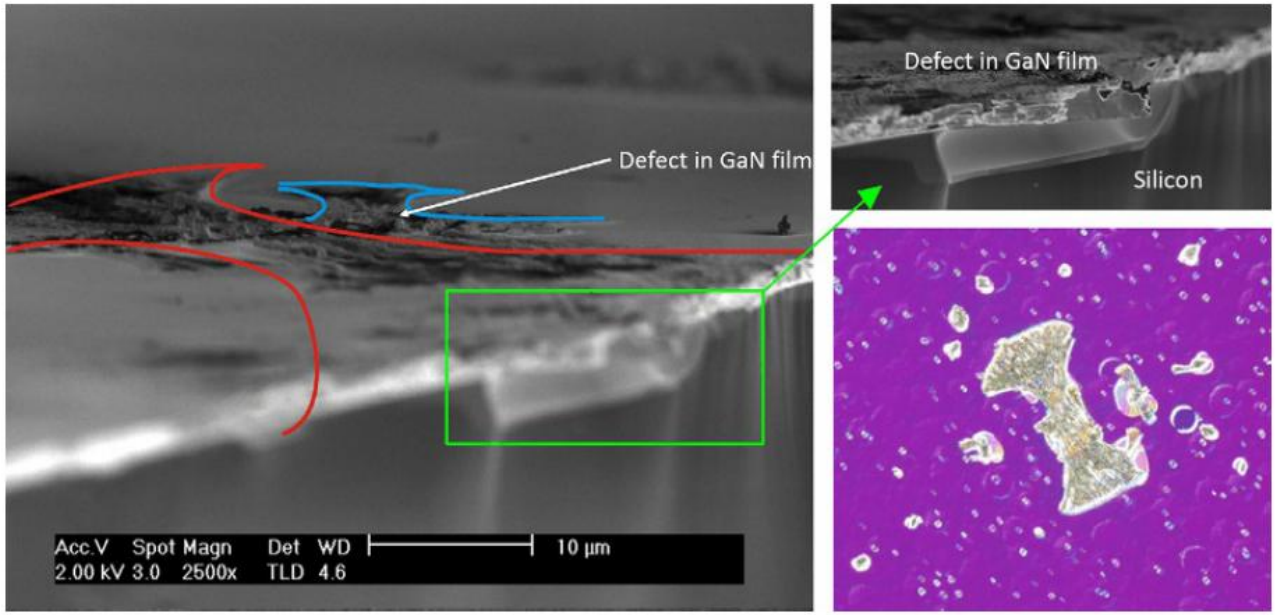
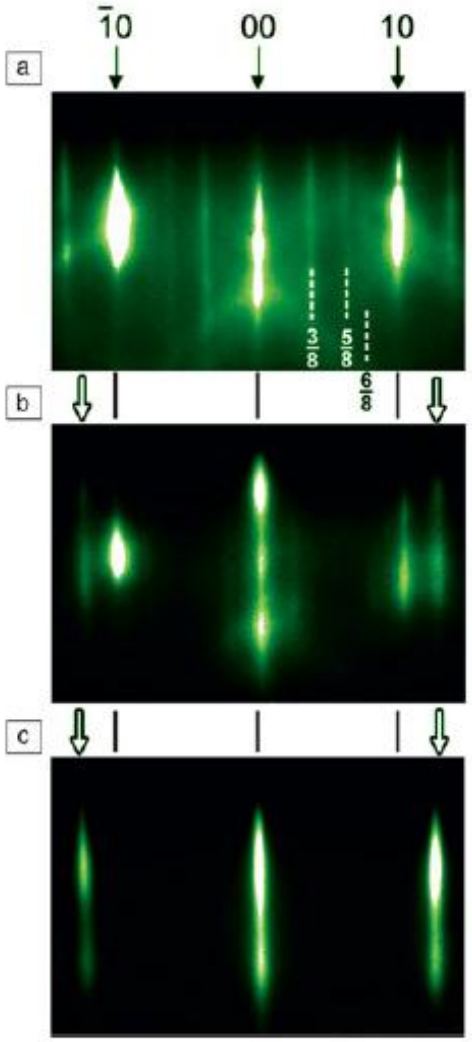


FIG. 4.2 Melt-back etching in silicon, with Nomarski image (bottom right), and etched hole in silicon as shown in the SEM images (left and top right). The *colored lines* show the outlines of the defects that are shown in the optical microscope image.

Chapter 4 – III-N Epitaxy on Si for Power Electronics
M. Charles, Y. Baines, E. Morvan and A. Torres
High Mobility Materials for CMOS Applications.
https://doi.org/10.1016/B978-0-08-102061-6.00004-5

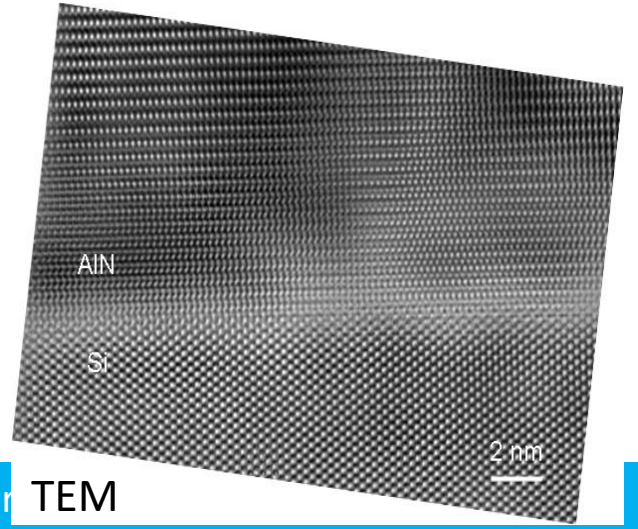
AlN Buffer Layer on Si by MBE

- **Nucleation process to obtain a sharp AlN/Si interface**

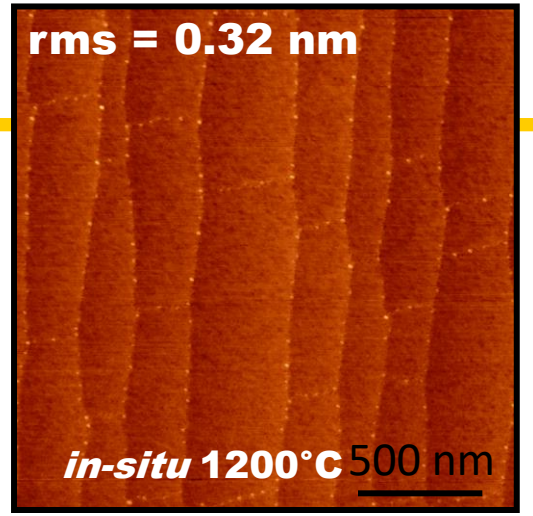


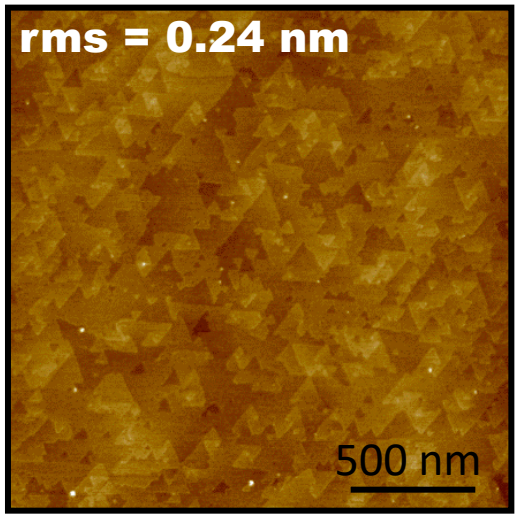
RHEED patterns along the [−110] azimuth of Si(111) during AlN nucleation using a NH_3-first nucleation process.
(a) after NH_3 pre-flow of Si(111) at 650°C and rapid thermal annealing at 820°C, a (8 × 8) surface reconstruction characteristic of β -Si_3N_4 (0001) surface is obtained.
(b) After deposition of 1 monolayer of Al at 650°C, the AlN(0001) (1 × 1) orders indicated by white arrows coexist with the Si(111) ones.
(c) after the growth of 40 nm AlN buffer layer at 920°C.

F. Semond , MRS BULLETIN
VOLUME 40, MAY 2015
DOI: 10.1557/mrs.2015.96



TEM





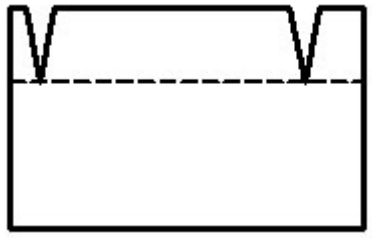
AFM

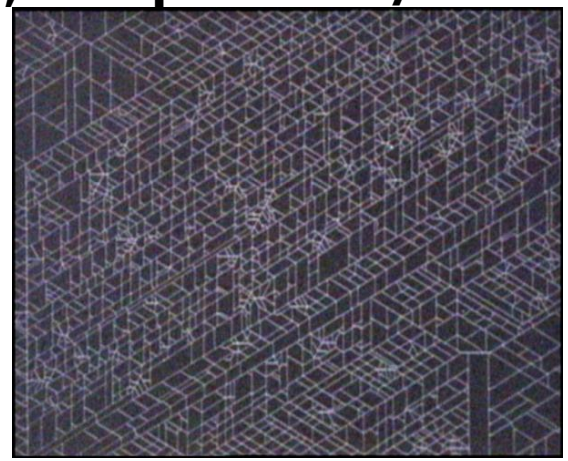
Hetero-Epitaxial Growth of GaN on Si

- **Main difficulties:**
  - **the melt-back etching --> reaction between Ga & Si at high temperature**
  - **high dislocation density --> lattice-mismatch**
  - **large stress --> thermal expansion coef. mismatch**

aGaN = 0.318 nm, $\alpha = 5.59 \times 10^{-6}\ K^{-1}$
aSi(111) = 0.384 nm, $\alpha = 3.59 \times 10^{-6}\ K^{-1}$
lattice-mismatch = 16.9%
TEC mismatch = 56%

Integration of GaN on silicon --> « manufacturability »
(compatibility of the wafers with a standard Si production line)
Low bow, low particule/defect count of the wafers & crack-free surface





Cracking of a GaN/Si structure due to the large tensile stress during the cooling process from growth temperature to room temperature originating from the TEC mismatch

Design of the Heterostructure

- **Integration of layers to control the strain:**

➡ **To grow crack-free GaN layers on Si,** it is necessary to maintain a certain amount of **compressive strain in GaN** in order to compensate for the tensile strain appearing during the post growth cooling from the growth temperature to room temperature.

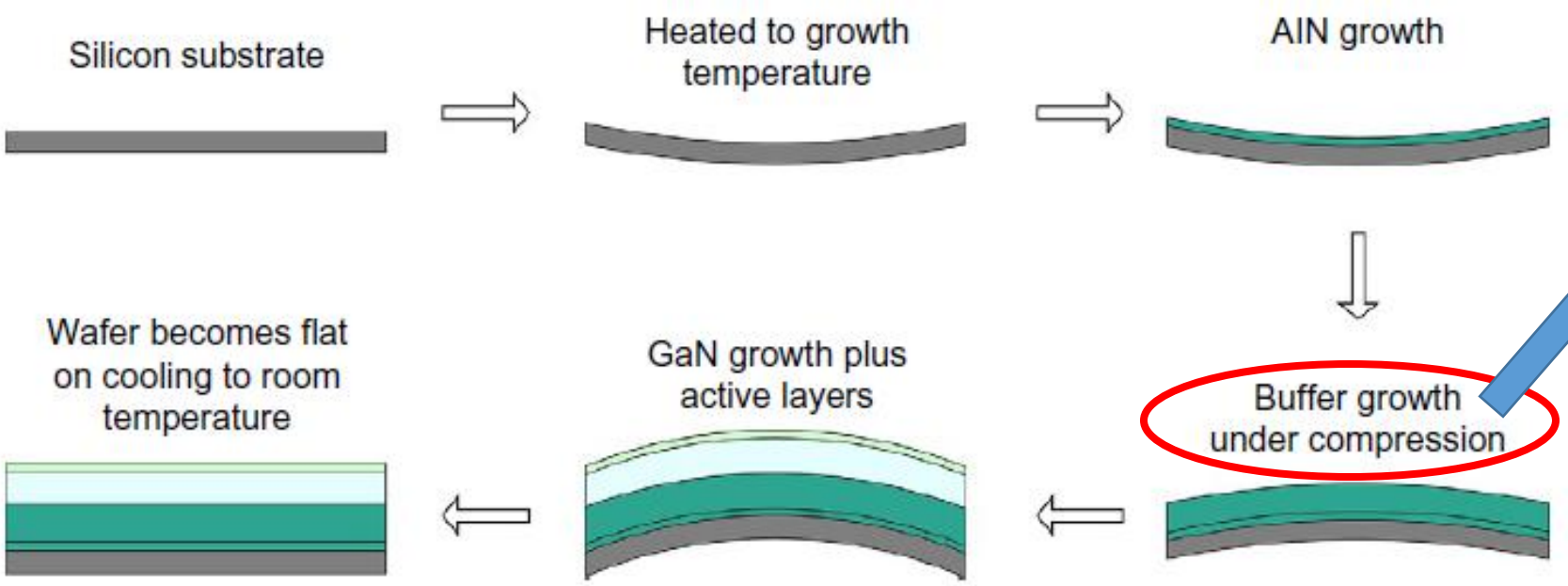


FIG. 4.4 Schematic of basic GaN-on-silicon growth.

Growth under compressive strain --> low Al content Layers on high Al content ones

to prevent cracking, **growth of GaN must be 2D**, which also means that **the surface morphology of the initial AlN or AlGaN buffer layer** needs to be as smooth as possible.

Design of the Heterostructure

➢ **Designing structures to preserve a compressive strain:**

1. Graded aluminum from AlN to GaN: with a smooth grading or a step grading of different $Al_xGa_{1-x}N$ layers

➡ to continually introduce compression into the layers.

2. AlN interlayers: after growing GaN on the Al(Ga)N nucleation layer, a new AlN layer is grown on this GaN layer. The AlN quickly reaches its critical strain thickness and then relaxes. After, **a GaN layer can be grown in compression** on the AlN layer.

➡ Presence of a strain gradient during the growth of the different layers (a slope of zero = fully relaxed structure)
Strong difference in the relaxation process between the first & second GaN layer → compressive strain of the structure

↪ **compensation of the tensile strain generated during the cooling process**

(In-situ curvature meas. gives the aver. deformation of the epitaxial structure)

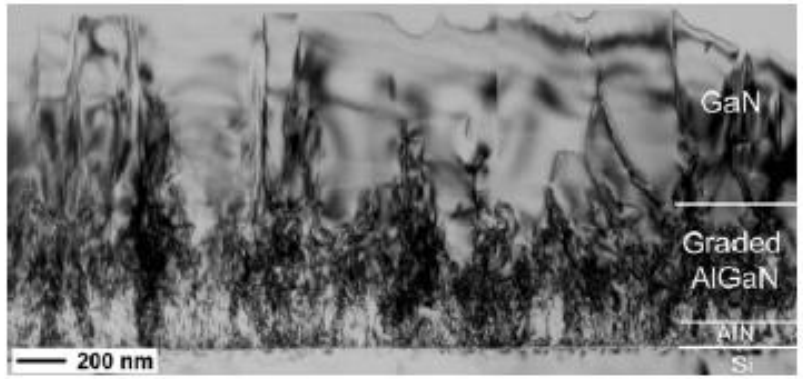
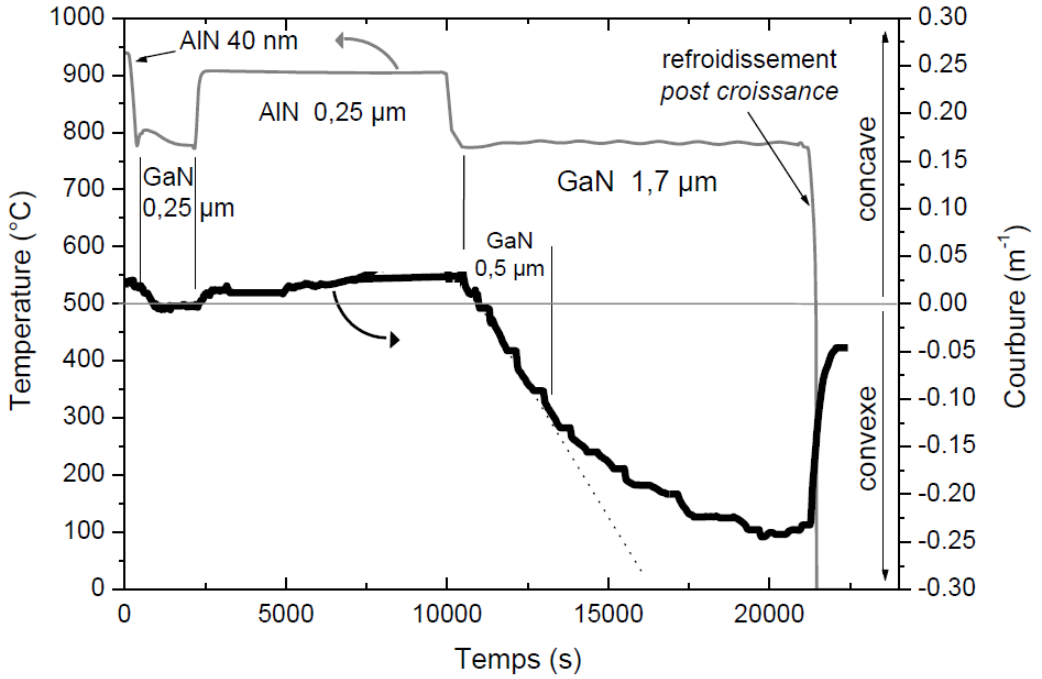


Fig. 7 Cross-sectional TEM image of GaN grown on the graded AlGaN buffer [39]

[B. Zhang et al., Chin. Sci. Bull. 1251 (2014)]



Design of the Heterostructure

➢ **Designing structures to preserve a compressive strain:**

1. Graded aluminum from AlN to GaN: with either a smooth grading or a step grading of different $Al_xGa_{1-x}N$ layers in order to continually introduce compression into the layers.

2. AlN interlayers: after growing GaN directly on the AlN nucleation layer, a new AlN layer is subsequently grown on this GaN layer. The AlN quickly reaches its critical strain thickness and then relaxes. After this, a GaN layer can once again be grown in compression on the AlN layer.

3. Thick superlattice structures: After the AlN nucleation layer, successive pairs of AlN and GaN (or AlGaN) are grown, with the AlN relaxing sufficiently to put the GaN in compression. The sum of the tension in the AlN and compression in the GaN gives a net addition of compression, and so, a large number of these repeats can be used to create thick structures, before the addition of a final GaN layer also in compression.

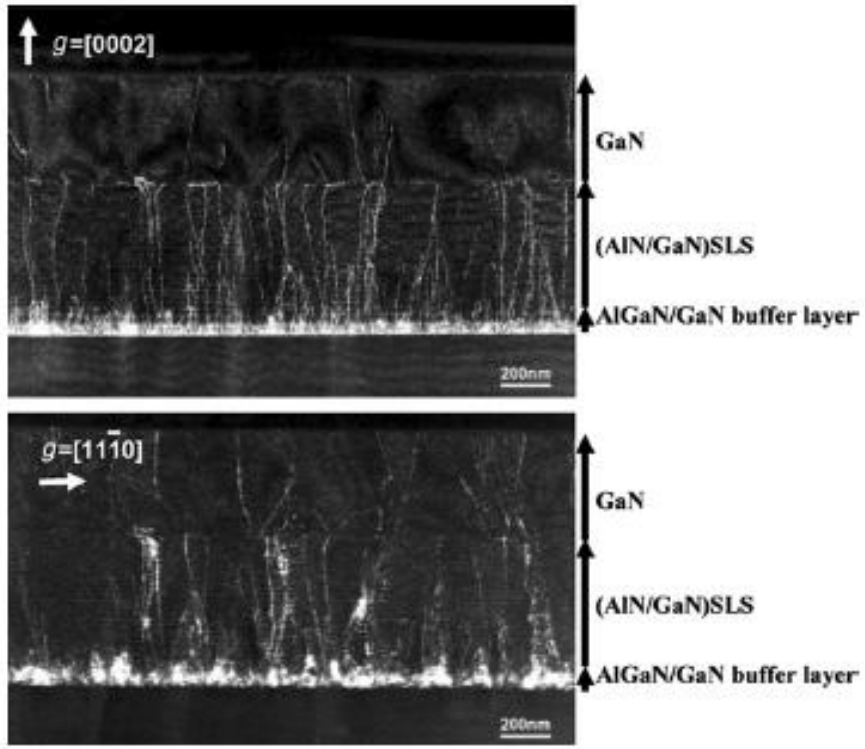


Fig. 6 Cross-sectional TEM image of GaN on Si [34]

[B. Zhang et al., Chin. Sci. Bull. 1251 (2014)]

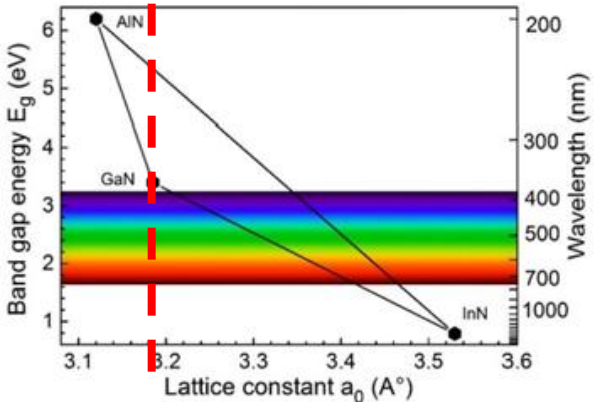
Effect of the Barrier Material

➢ **Designing structures to improve the HEMT characteristics:**

1. The AlGaN/AlN/GaN double heterojunction with the insertion of a thin AlN layer of the order of 1nm between the AlGaN barrier and the GaN channel. **The AlN "spacer" layer allows more e- to accumulate in the GaN channel combined with better confinement due to the larger band offset which increases the mobility.**

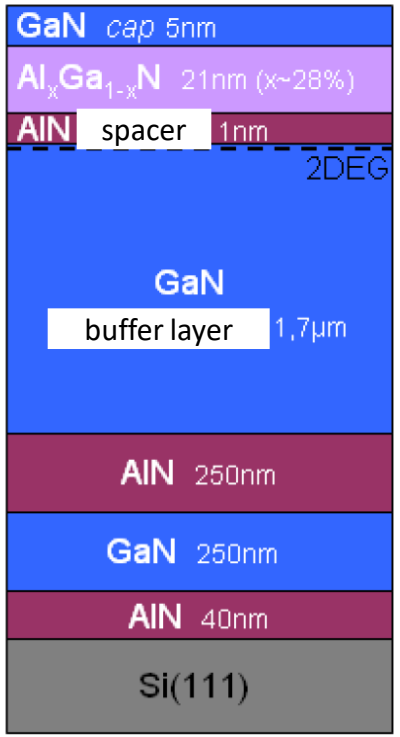
This gives lower sheet resistance: $$R_{sh} = \frac{1}{e\mu N_s}$$

2. Design of the AlGaN capping with larger Al content or lattice-matched AlInN to reach larger Ns values.



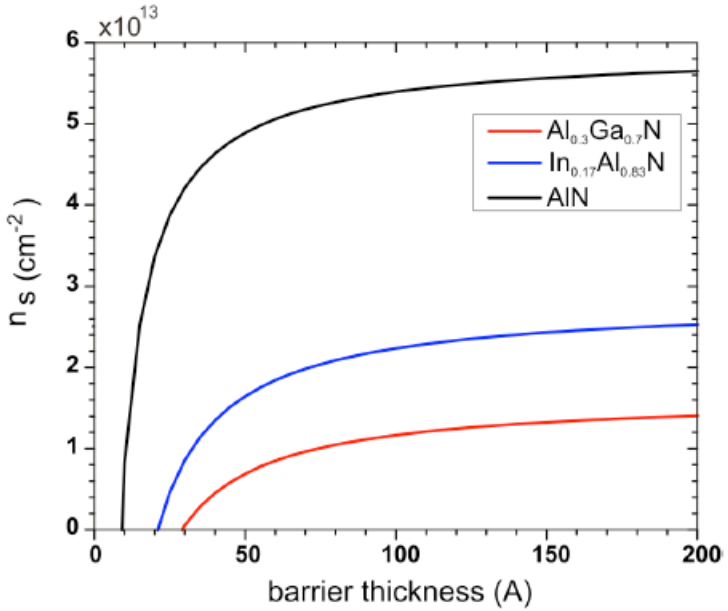
Mobility μ > 1800 cm².V⁻¹.s⁻¹
Sheet carrier density > 1x10¹³ cm⁻²
@ 300K

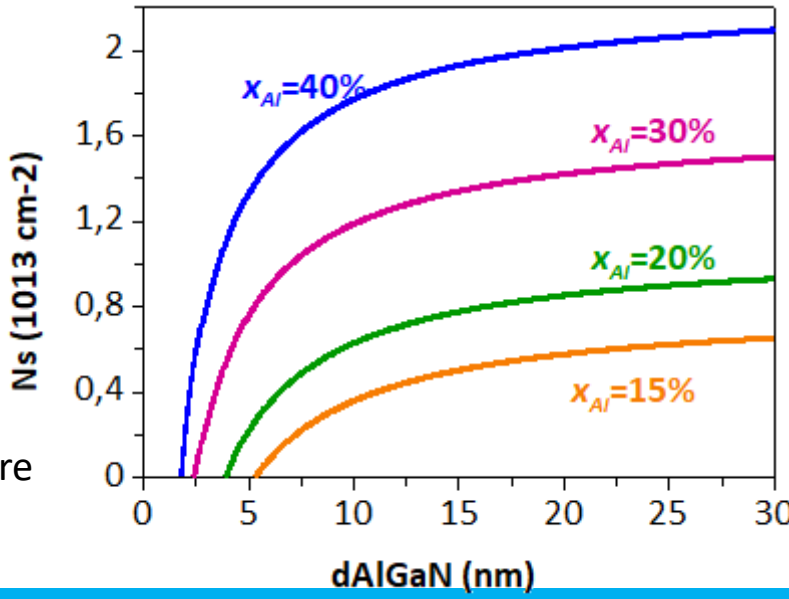
[Y. Cordier et al., III-Nitride Semiconductors & their Modern Devices, 2013)]



Schematic of a typical AlGaN/GaN HEMT structure

[N. BARON, thèse, Univ. Nice (2009)]





[S. RENNESSON, thèse, Univ. Nice (2013)]

Combining MBE & MOCVD

➢ **AlGaN/GaN HEMTs on Si**

One of the challenges is the vertical voltage-blocking capability of the GaN-on-Si epitaxial stack which limits the maximum voltage operation.

➡ Vertical buffer current is correlated to charge injection from the Si substrate

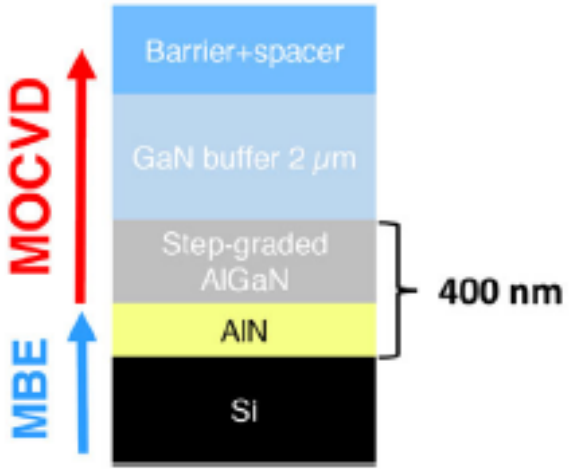
--> **a parasitic channel forming between the AlN nucleation and the Si.**

➢ Suppression of the formation of this channel --> ↙ AlN growth temperature

↪ Limit in MOCVD growth due to severe material quality degradation.

➢ **Hybrid growth approach**

➡ Combining the use of MBE AlN nucleation layer @ LT with a MOCVD HEMT structure.



Coll. CRHEA – Aachen Univ. & Magdeburg Univ.

[H. Yacoub et al., Phys. Status Solidi A, 1700638(2018)]

Combining MBE & MOCVD

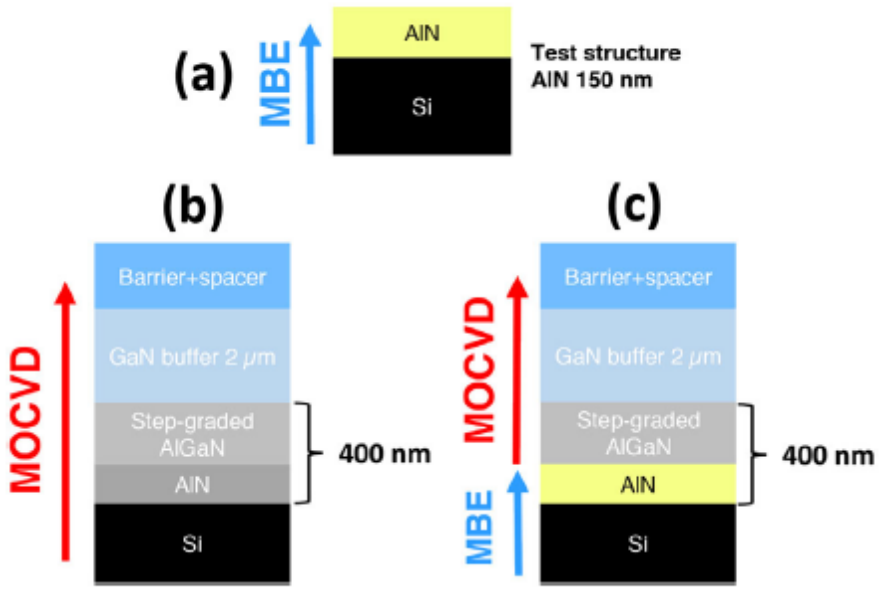


Figure 1. Schematic showing epitaxial layer structure for (a) MBE AlN-on-silicon test structure, (b) MOCVD HFET and (c) hybrid MBE/MOCVD HFET structures on silicon.

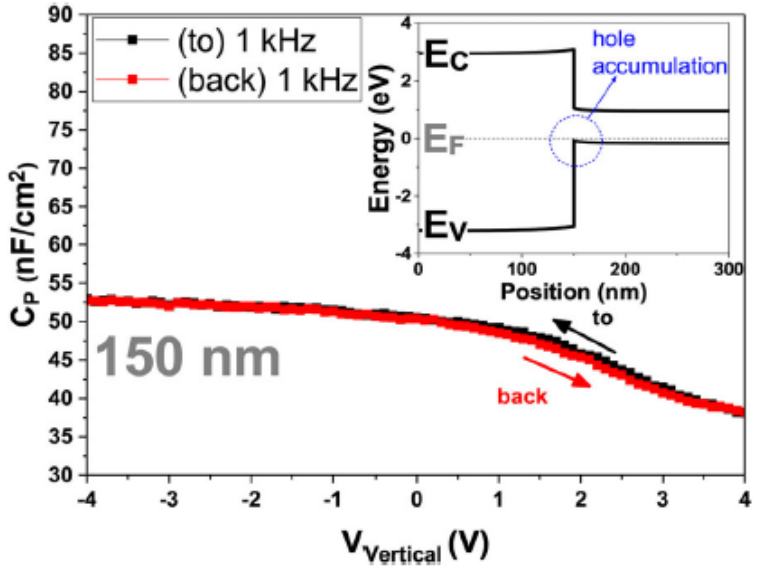


Figure 3. C-V measurements performed on 150 nm AlN/Si test structures. Bias was swept from 4 to −4 V and back at a measurement frequency of 1 kHz. Inset shows simulated 0 V band diagram for 150 nm AlN on Si indicating hole accumulation at the interface.

[H. Yacoub et al., Phys. Status Solidi A, 1700638(2018)]

- **C–V measurements on 150nm MBE AlN/p-Si test structures**

→ @ 0V: hole accumulation is still observed and the capacitance decreases until 4V. No further increase in Cp is observed at higher positive biases, **indicating the suppression of e- accumulation at the interface** (an increase in the positive bias voltage regime initiated by carrier injection originating from an inversion channel formed between AlN and the p-Si substrate). **This e- channel is responsible for the vertical leakage current in the buffer structure**.

→ **C–V profile shows no hysteresis** (between to/back-sweeps): **high AlN/Si interface quality.**

Combining MBE & MOCVD

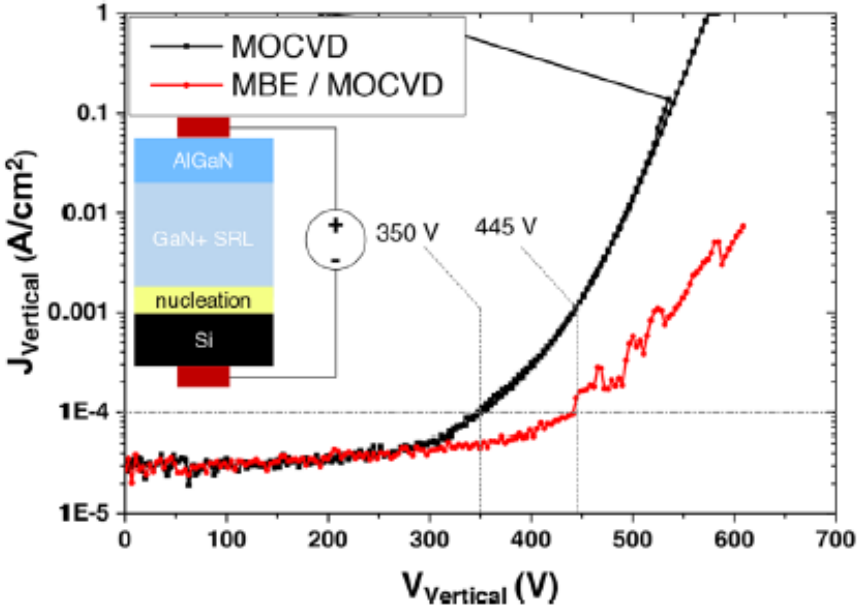


Figure 6. Vertical buffer leakage current for hybrid MBE/MOCVD (red) and MOCVD (black) samples. Inset showing measurement setup.

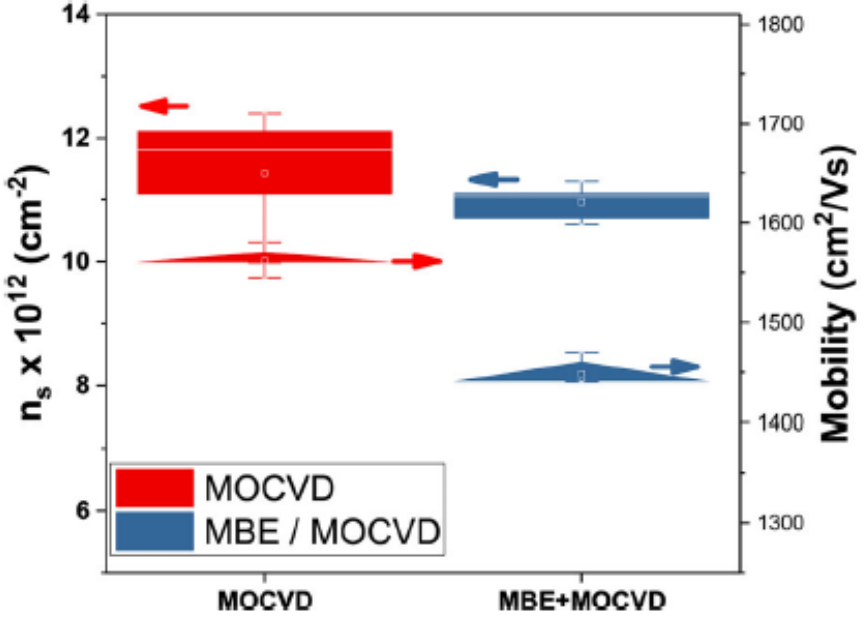


Figure 7. Carrier density and mobility obtained for both samples from Hall measurements.

- **Vertical buffer leakage (I–V): MOCVD-sample shows 1x10^{-4} Acm^{-2} current density @ 350V & hybrid MBE/MOCVD-sample has the same J @ 445 V yielding an increase of 27%.**

➡ **The hybrid growth reduces the vertical buffer current. The initial growth conditions impact the voltage-blocking capabilities** (@ 600 V 100x lower J for MBE/MOCVD structure).

- **Hall meas.: slight decrease in the channel mobility for MBE/MOCVD-sample. The mean carrier concentrations are similar --> 2DEG properties of the samples are comparable.**

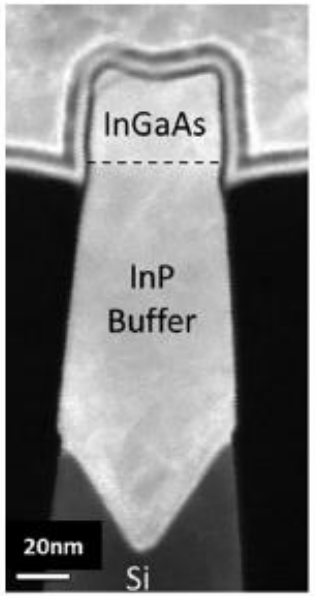
Perspectives & Challenges

- **Monolithic integration of III-V SC on Si attracts a lot of interest to benefit from the superior electron mobility / high saturation velocity / high temperature / high power**

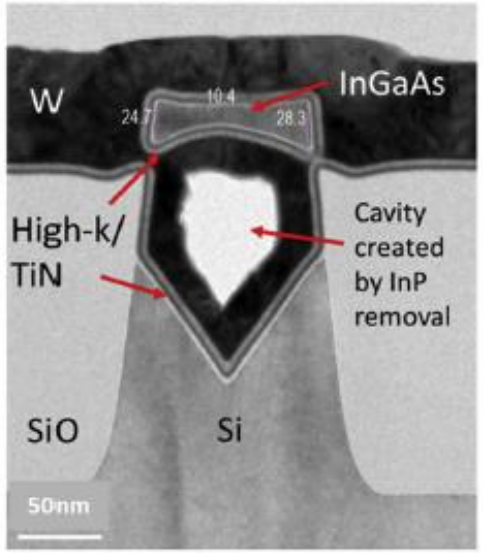
- **Important improvements & achievements with demonstration of fully integrated III-V devices on 300 mm Si substrates in a VLSI compatible flow**

[N. Waldron et al., Solid-State Electronics 115, 81 (2016)]

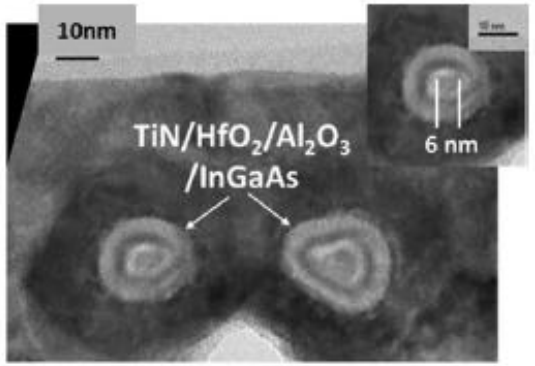
Fin FET



Gate All Around



Nanowires



direct optical band gap offers the possibility to integrate light sources on Si for optical interconnections

- **Challenges still exist:**

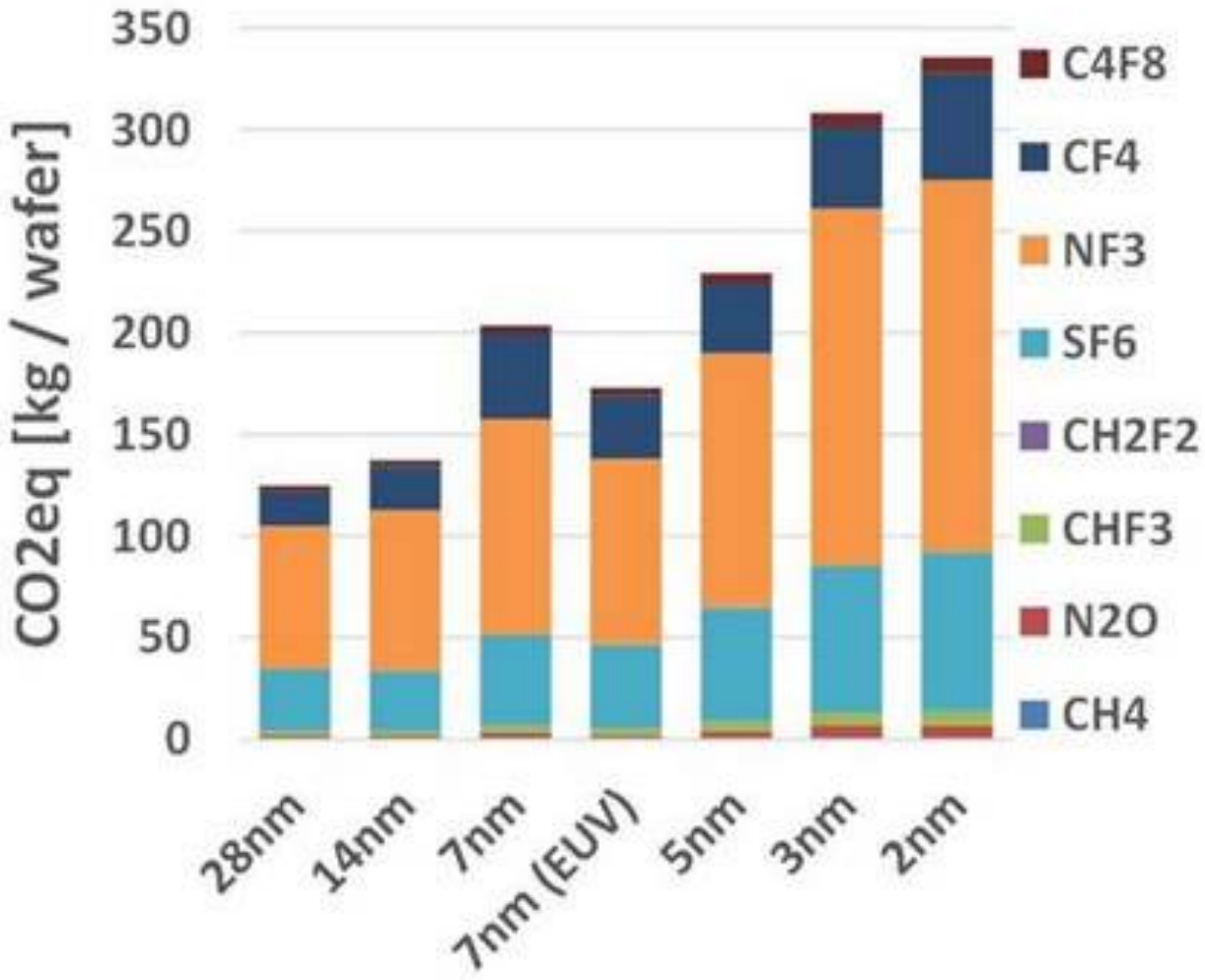
  → **Control of the defects in heteroepitaxy** (lattice mismatch) (III-V, IV-IV) **in a compact volume, compatible with Si CMOS devices.**

- **In the longer term, new beyond-CMOS materials like CNTs and 2D materials may add further to the material palette for heterogeneity and new nanosystems.**

Environmental Impact

- **Environmental footprint of CMOS technologies**

  https://www.imec-int.com/en/articles/environmental-footprint-logic-cmos-technologies



Estimated equivalent CO2 emissions from greenhouse gases used in process flows across different nodes.

Thank you for your attention

Transistor: Advantages & Challenges

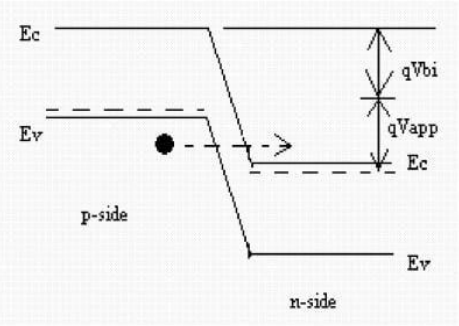
Transistor	Advantages	Challenges
FinFET	Mainstream CMOS	Scalability
FDSOI	Unique back bias capability	Scalability Low drive current per unit area
Horizontal nanowire	Great electrostatics	Parasitic capacitance
Nanosheet	Good tradeoff between electrostatics and parasitics	Scalability
Vertical nanowire	Great electrostatics Good scalability	Unique process challenges
Germanium / III-V	Higher carrier mobilities than Si	Material defects Gate stack Contact resistance
CNT / 2D semiconductor / Graphene	Superior electrostatics / carrier mobilities	Material defects Gate stack Contact resistance Compatibility with silicon

[K. Cheng et al., ECS Transactions 80, 17 (2017)]

Issues for nanoscale MOSFET (1)

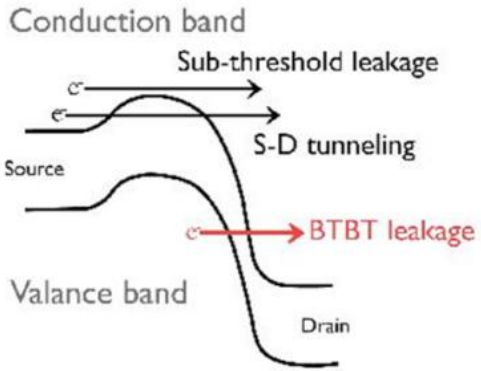
➢ Reverse bias-pn junction leakage current

For heavily doped pn junction of drain/source and substrate regions, the band-to-band tunneling (BTBT) effect dominates the reverse bias leakage current. In band-to-band tunneling, electrons tunnel directly from the valence band of the p region to the conduction band of the n region.



➢ Subthrehold leakage current

When $0 < V_{GS} < V_{th}$: the transistor is biased in the subthreshold or weak inversion region and the concentration of minority carriers is small but not zero.

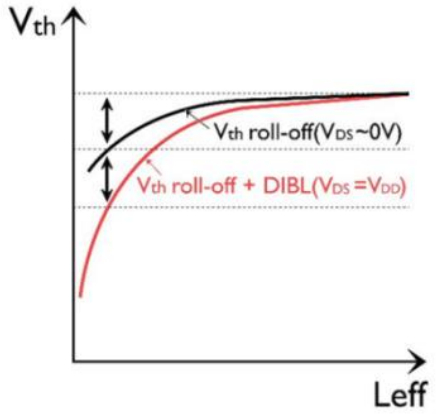


➢ Drain-Induced Barrier Lowering (DIBL)

Subthreshold leakage current is mainly due to drain-induced barrier lowering. In short channel devices, the depletion region of drain and source interact with each other and reduce the potential barrier at the source. The source is then able to inject charge carriers into the surface of the channel resulting in subthreshold leakage current (pronounced in high drain voltages and short channel devices).

➢ V_{th} Roll Off

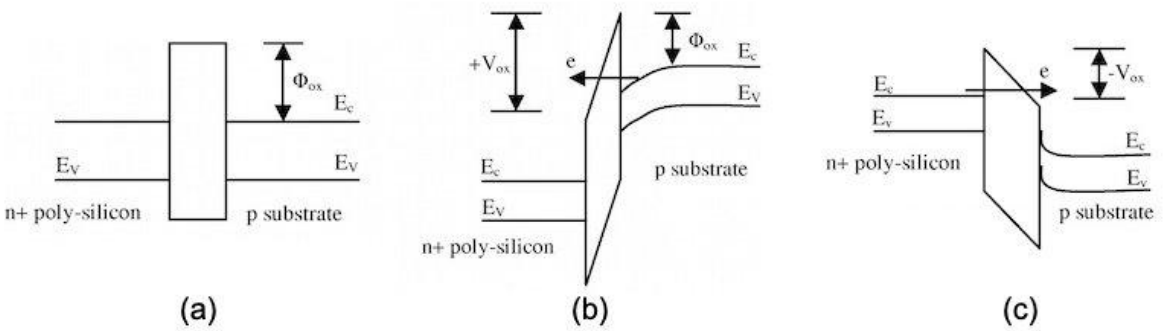
Vth reduces due to channel length reduction. The drain and source depletion region enter further into the channel length, depleting a part of the channel. Due to this, a lesser gate voltage is required to invert the channel reducing the threshold voltage. The reduction in threshold voltages increases the subthreshold leakage current as the subthreshold current is inversely proportional to the threshold voltage.



Issues for nanoscale MOSFET (2)

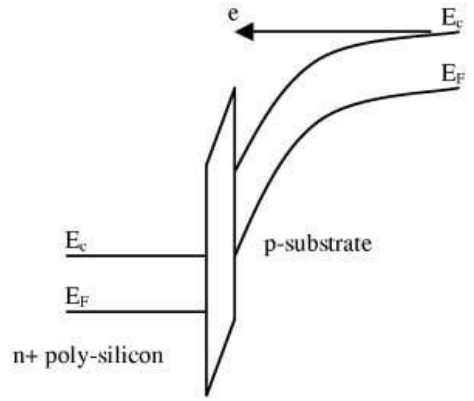
➢ Tunneling into and Through Gate Oxide Leakage Current

A thin gate oxide results in high electric fields across the SiO_2 layer. Low oxide thickness with high electric fields results in electrons tunneling from the substrate to the gate and from the gate to the substrate through the gate oxide, resulting in gate oxide tunneling current.



➢ Leakage Current Due to Hot Carrier Injection from the Substrate to Gate Oxide

The high electric field near the substrate-oxide interface energizes the electrons or holes and they cross the substrate-oxide interface to enter the oxide layer. This phenomenon is known as hot carrier injection. This phenomenon is more likely to affect electrons than holes. This is because electrons have a lesser effective mass and a lesser barrier height as compared to holes.



➢ Leakage Current Due to Punch-Through Effect

Due to the proximity of drain and source terminals, the depletion region of both the terminals come together and eventually merge. In such a condition, "punch-through" is said to have taken place. The punch-through effect lowers the potential barrier for the majority of carriers from the source. This increases the number of carriers entering into the substrate. Some of these carriers are collected by the drain and the rest contribute to leakage current.

https://www.allaboutcircuits.com/technical-articles/6-causes-of-mos-transistor-leakage-current/