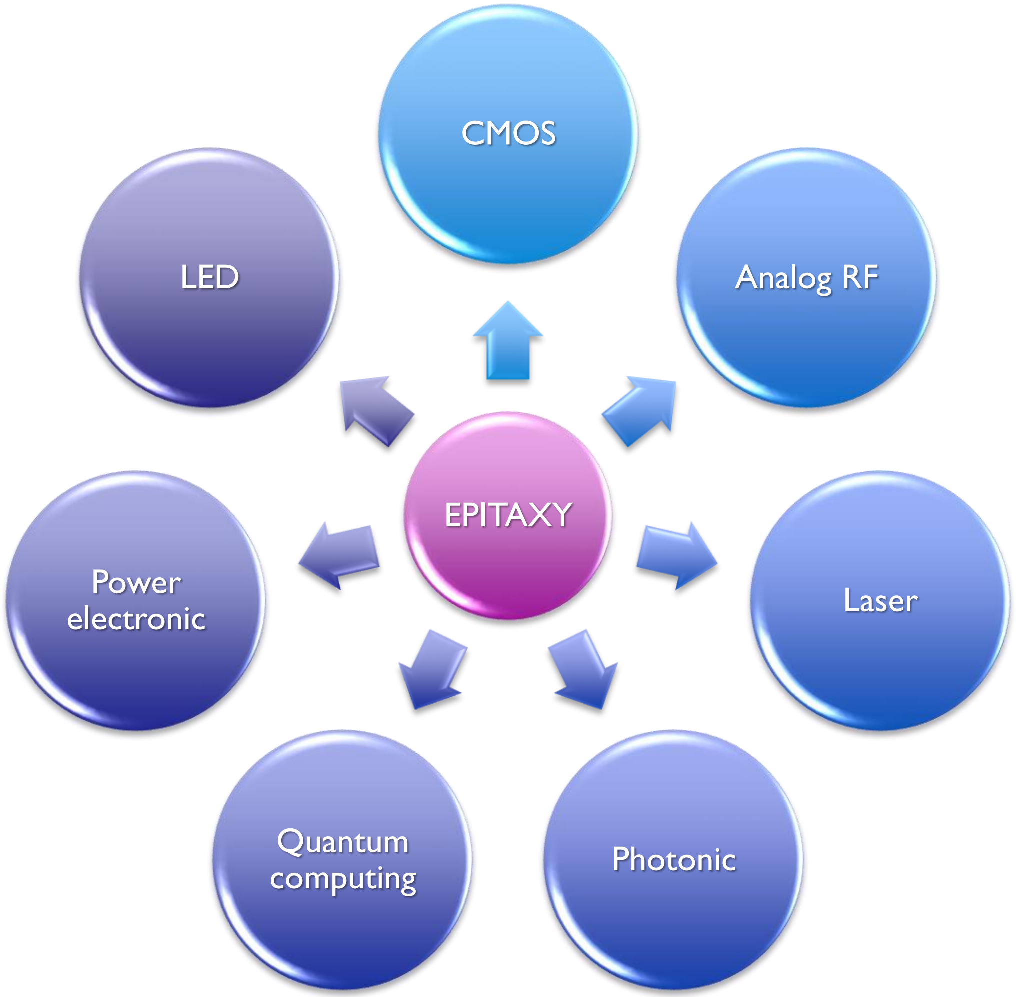
Table ronde "recherche fondamentale - industrie"

Prof. Dr. Clement MERCKLING

08/07/2021

Epitaxy @ center of technologies



PHYSICAL REVIEW LETTERS **121,** 166101 (2018)

Editors' Suggestion | Featured in Physics

Atomic Step Flow on a Nanofacet

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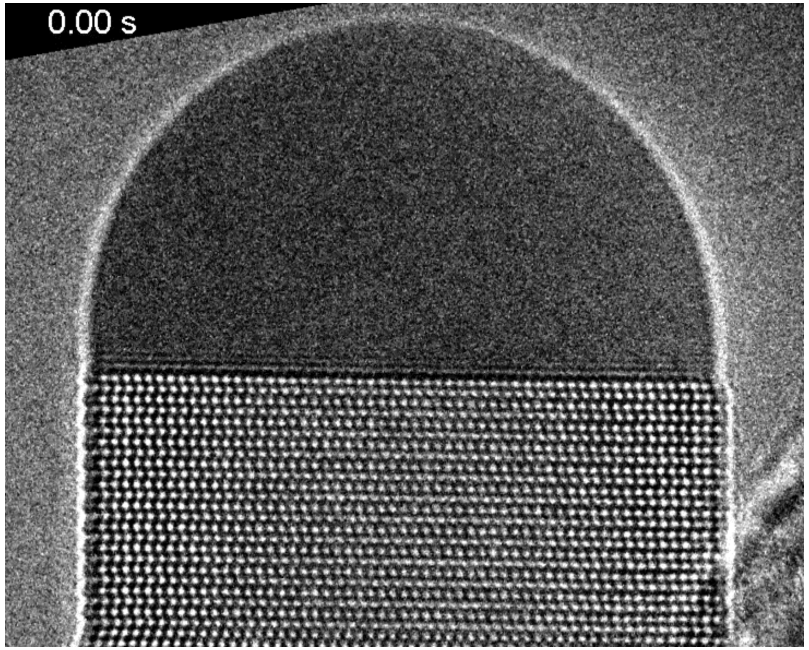
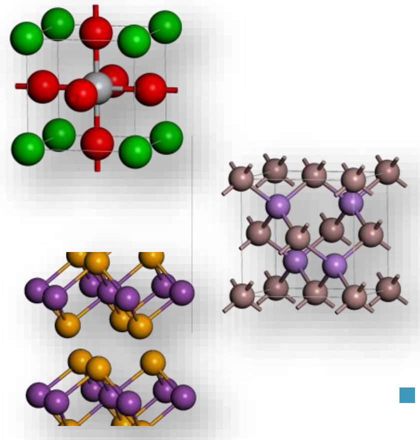
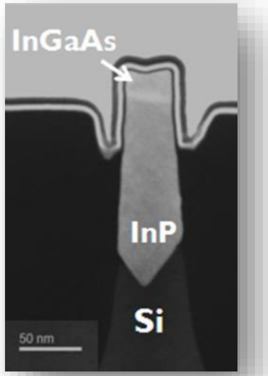


public

Personal experience

- Core competence: Crystal growth (epitaxy) of thin films at atomic scale
  - Started epitaxy in 2004 (INL / ST)
  - Pursued at imec since 2007
- Technics
  - MBE, MOVPE, PLD
- Characterizations
  - RHEED, XRD, PL, AFM, XPS, ARPES, …
- Materials
  - Crystalline oxides
  - Semiconductors
  - Van der Waals compounds
  - Surfaces & interfaces science





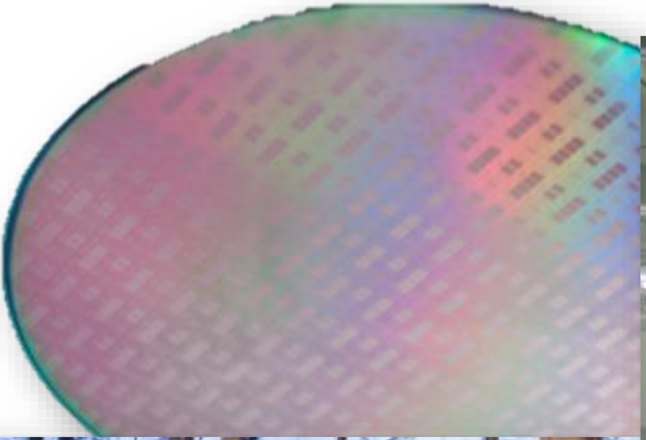
- Additional skills
  - ab-initio simulations
  - Devices & applications
    - Logic, Photonic, Quantum, …
- Scientific communications
  - h-index = **35**
  - # total peer review publications: **155**
    - # first author publications: **22**
    - # last author publications: **11**
  - # patents: **15**
  - # book chapter: **1**
  - # invited talks in international conferences: **15**
- Mentoring & Leadership

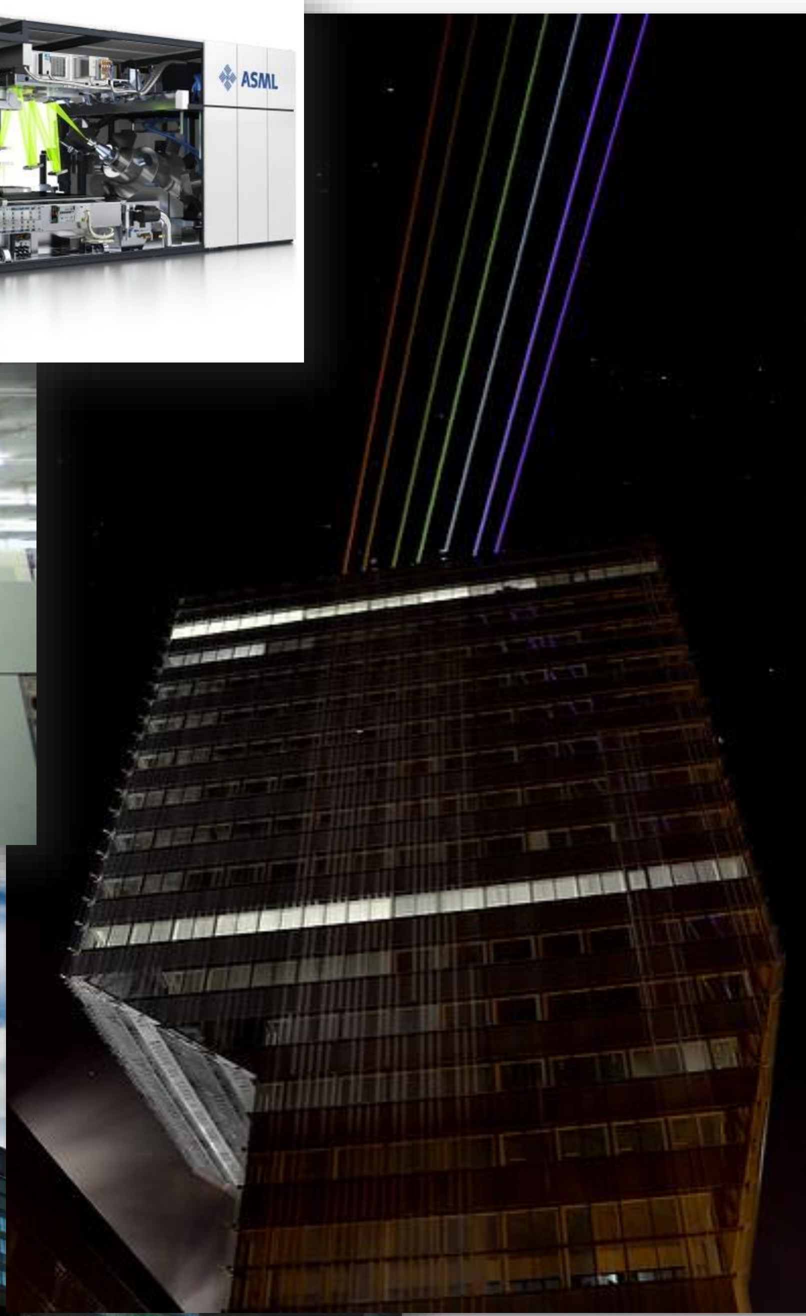
Imec in a nutshell

- imec
  - Started in 1984 (initial staff: 70 persons)
  - 5000 imec'ers
  - 74 Nationalities
  - Worldwide implantation
- Finances
  - > 700 M€
  - ~15% Flanders government
- Main activity
  - R&D and innovation hub in nanoelectronics and digital technology
- Core competences
  - Driving microchip miniaturization
  - Internet of everything
    - Smart health
    - Smart automotive
    - Smart city
    - Smart technology
    - Smart energy

public

imec

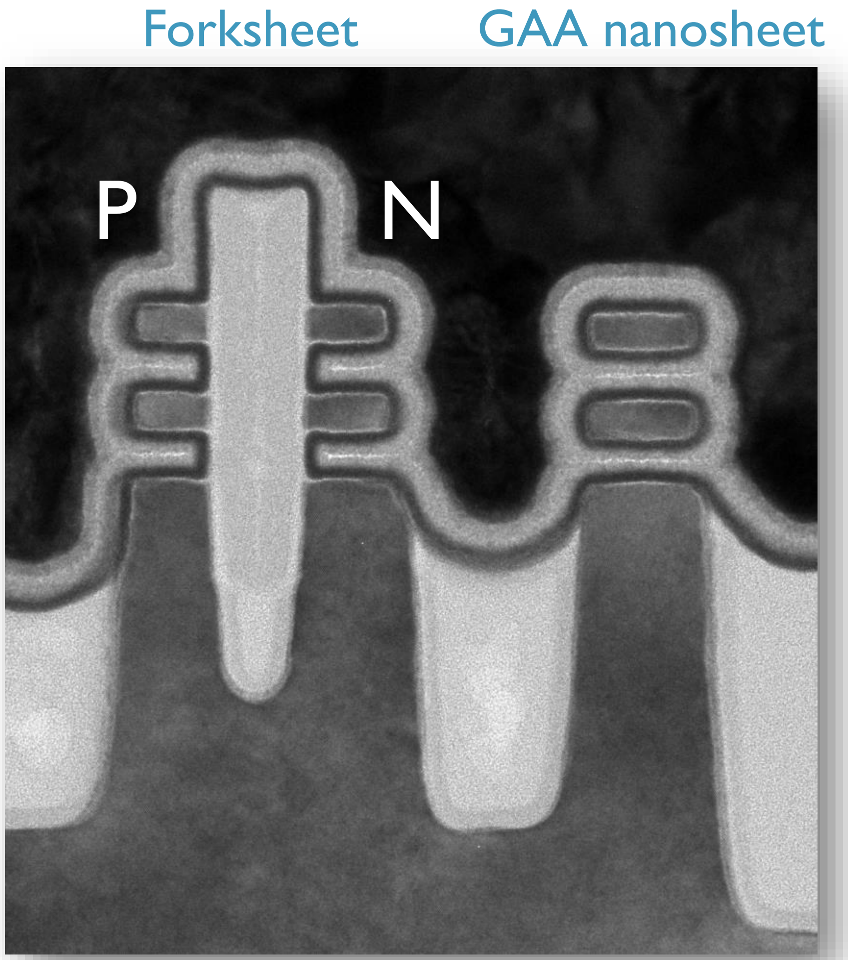




Advanced CMOS

SiGe

- The forksheet device has recently been proposed as the most promising device architecture to **extend the GAA nanosheet** device generation with additional scaling and performance beyond 2nm technology node.
- Unlike nanosheet devices, the sheets are now controlled by a **tri-gate forked structure** – realized by introducing a *dielectric wall* in between the p- and nMOS devices before gate patterning. This wall physically isolates the p-gate trench from the n-gate trench, allowing a much **tighter n-to-p spacing** than what is possible with either FinFET or nanosheet devices.

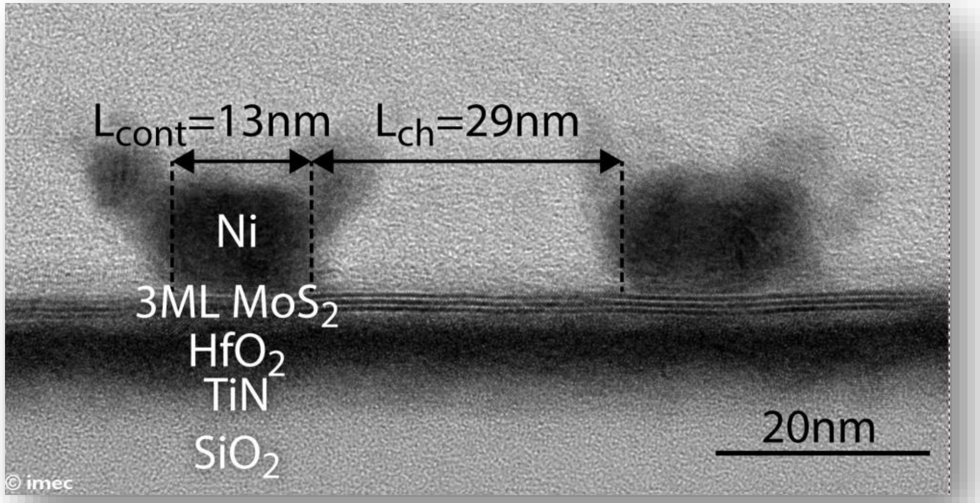


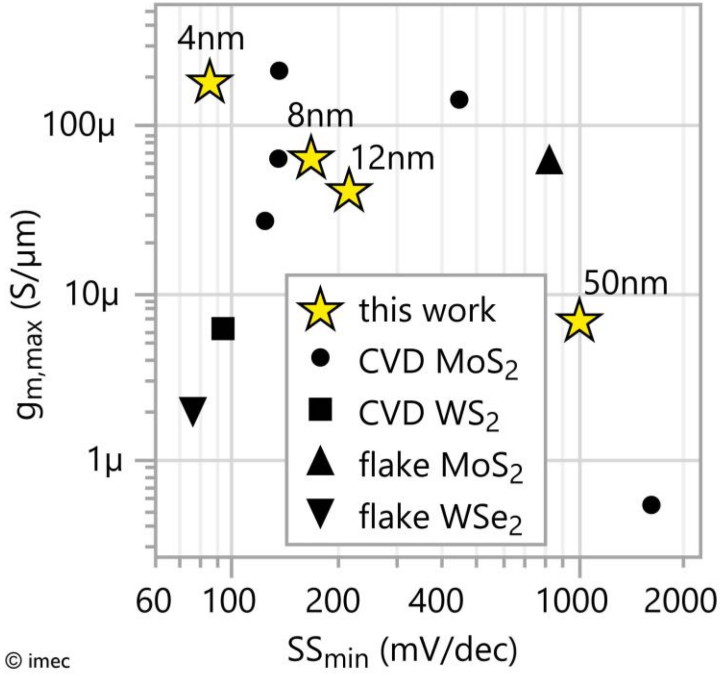
https://www.imec-int.com/en/press/imec-reports-first-electrical-demonstration-integrated-forksheet-devices-extend-nanosheets

Beyond CMOS

2D materials

- MoS_2 is a 2D material, meaning that it can be grown in stable form with nearly **atomic thickness** and atomic precision.
- Imec synthesized the material down to monolayer (0.6nm thickness) and fabricated devices with **scaled contact** and **channel length**, as small as 13nm and 30nm respectively.
- These very scaled dimensions, combined with **scaled high-k oxide gate thickness**, have enabled the demonstration of some of the best device performances so far.

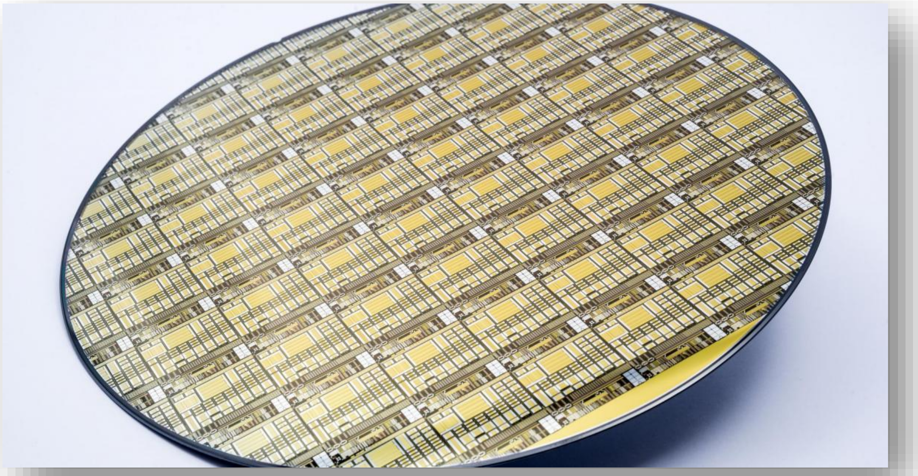


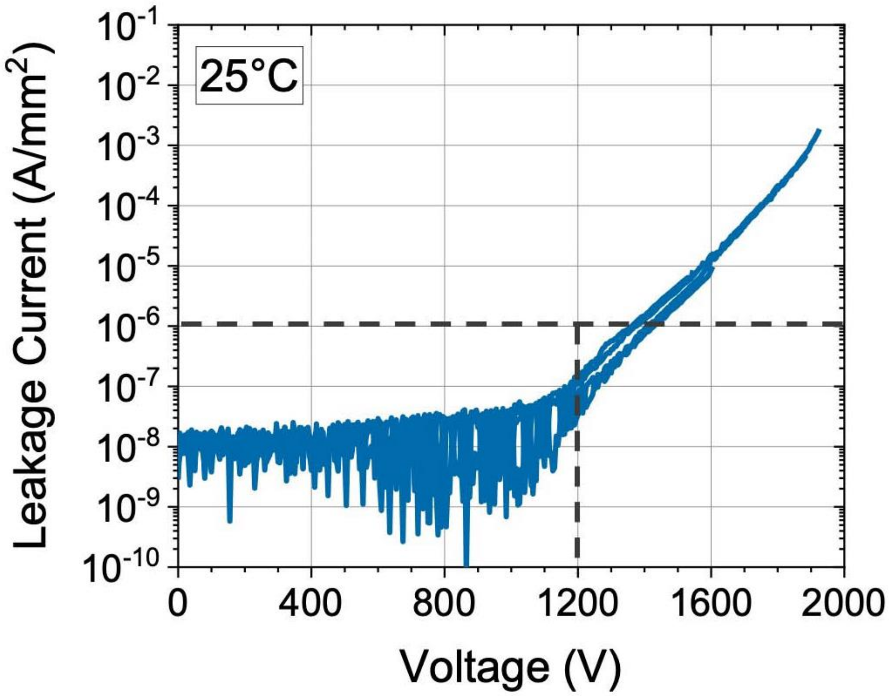


https://www.imec-int.com/en/articles/imec-shows-excellent-performance-in-ultra-scaled-fets-with-2d-material-channel

Power electronic
GaN

- Wide-bandgap materials gallium-nitride (GaN) and silicon-carbide (SiC) have proved their value as next-generation semiconductors for **power-demanding applications**.
- SiC-based technology is the most mature, but it is also more **expensive**. Over the years tremendous progress has been made with GaN-based technology grown on for example 200mm Si wafers.
- However, achieving operating voltages higher than 650V has been challenged by the difficulty of **growing thick-enough GaN buffer** layers on 200mm wafers.
- The manufacturability of 1200V-qualified buffer layers opens doors to highest voltage GaN-based power applications such as electric cars, previously only feasible with silicon-carbide (SiC)-based technology.

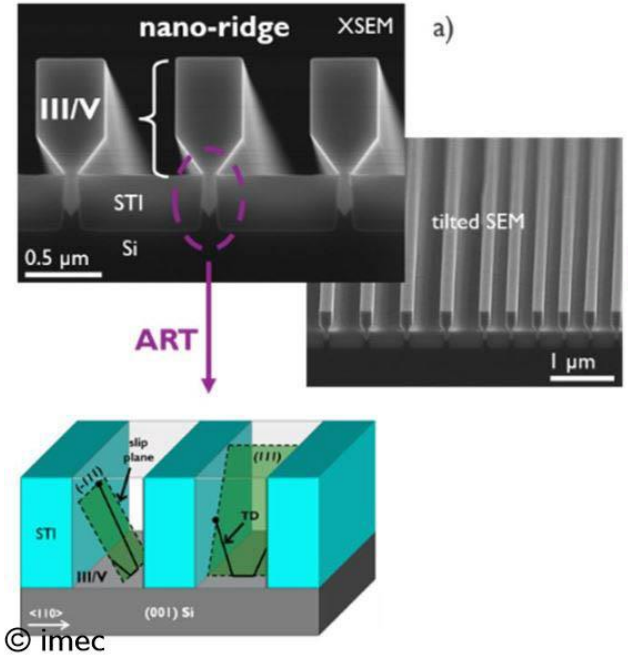


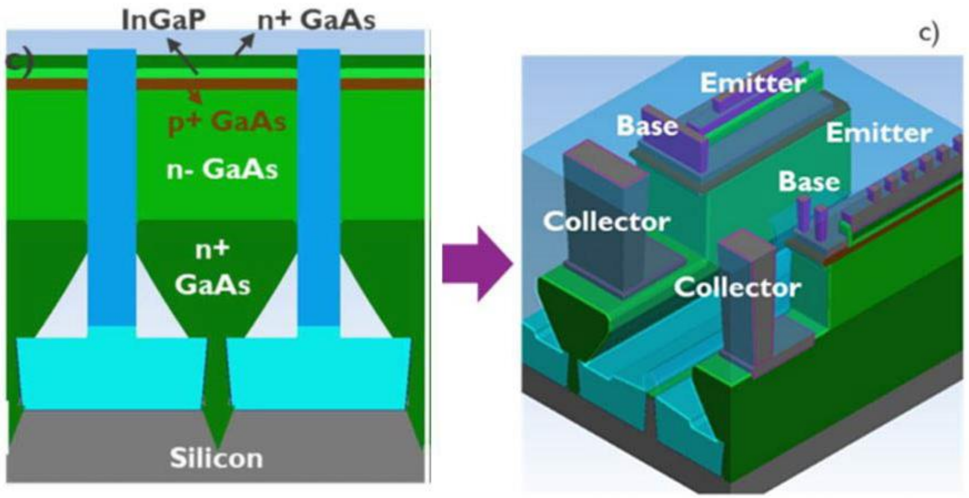


https://www.imec-int.com/en/press/imec-and-aixtron-demonstrate-200-mm-gan-epitaxy-aix-g5-c-1200v-applications-breakdown-excess

Beyond 5G RF Front-End Modules
III-V's

- To enable the next-generation **RF front-end modules** beyond 5G, imec explores CMOS-compatible III-V-on-Si technology
- Functional GaAs/InGaP HBT devices grown on 300mm Si have been demonstrated as a first step towards the enablement of InP-based devices.
- A low defect density device stack with below $3x10^{6}$ cm^{-2} threading dislocation density was obtained by using **III-V nano-ridge engineering** (NRE) process.
- The devices perform considerably better than reference devices, with GaAs fabricated on Si substrates with strain relaxed buffer (SRB) layers.



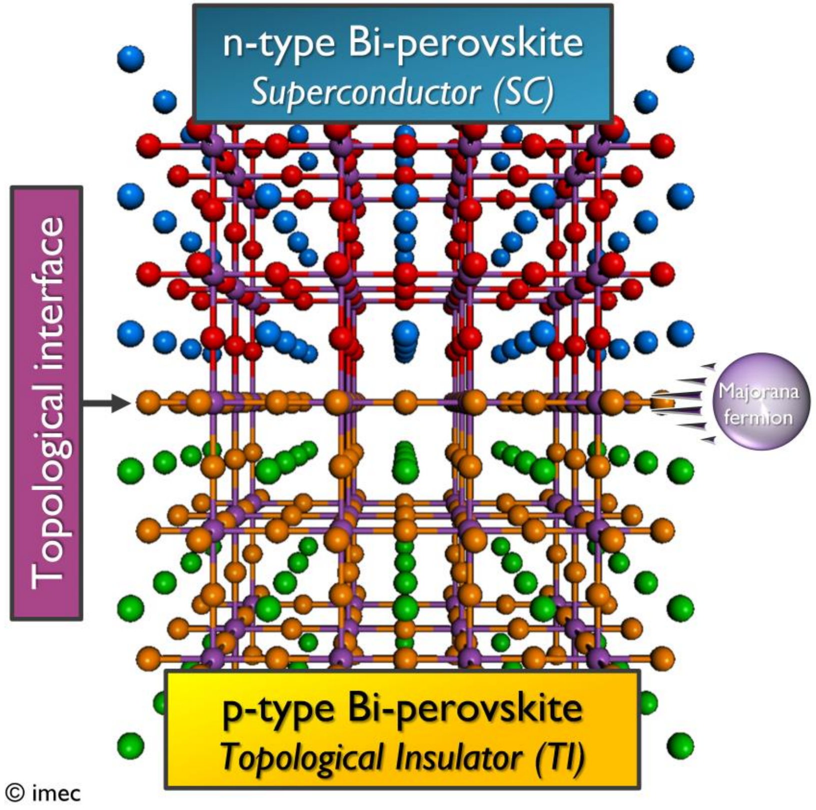


https://www.imec-int.com/en/articles/imec-demonstrates-scalable-iii-v-and-iii-n-devices-on-si-targeting-beyond-5g-rf-front-end-modules

Quantum computing

Oxides

- Within the project called NOTICE (for Novel Oxides and Topological Interfaces for quantum Computing Electronics), we follow an innovative route for generating **Majorana fermions**.
- This route will answer today's major blocking points, being the stability and oxidation of the SOC materials, and the **defectivity of the interface** between the SOC and superconducting materials.
- Groundbreaking idea is to use novel and **stable oxide materials** – i.e., a bismuth-based 'perovskite' oxide – as the basis for both the **superconductor** (by p-type doping) and **topological insulator** (by n-type doping).
- This material system combination is expected to create a perfect epitaxial interface, at which the Majorana fermions will be generated.



https://www.imec-int.com/en/articles/prestigious-european-erc-consolidator-grant-awarded-to-imec-s-clement-merckling-for-developing-fault-tolerant-qubits embracing a better life